A 148 $f_s$ rms Integrated Noise 4MHz Bandwidth All-Digital Second-Order $\Delta \Sigma$ Time-to-Digital Converter Using Gated Switched-Ring Oscillator

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Abstract—This paper presents an all-digital second-order $\Delta \Sigma$ time-to-digital converter (TDC) by using switched-ring oscillator (SRO) and gated switched-ring oscillator (GSRO). Unlike conventional multi-stage noise-shaping (MASH) TDC using the SRO, the proposed TDC does not require complex calibration to compensate for the error from frequency difference between the SROs. The prototype TDC achieves 148 $f_s$ rms integrated noise and 80.4dB dynamic range in 4MHz signal bandwidth at 400MS/s while consuming 6.55mW in a 65nm CMOS process.

I. INTRODUCTION

High resolution time-to-digital converters (TDCs) are employed in digital PLLs, time-domain ADCs, jitter measurement and time-of-flight detection [1]–[3]. For low-bandwidth applications, $\Delta \Sigma$ TDCs exploiting noise-shaping property have been proposed to achieve high-resolution, high linearity. In [4], a GRO-TDC has been introduced as a first-order $\Delta \Sigma$ TDC, achieving picosecond time-resolution with 90dB dynamic range. Unfortunately, over-sampling ratio (OSR) of a GRO-TDC is limited by the input pulse rate ($f_i$) since sampling frequency ($f_S$) must be the same as $f_i$. Thus, the time-resolution is limited if the input pulse rate is low. To achieve high OSR for low input pulse rates, an SRO-TDC [5] was proposed, where $f_s$ can be higher than $f_i$, resulting in a finer time-resolution. To further improve the time-resolution and signal bandwidth, a second-order MASH TDC using SROs has been proposed [8] since the OSR cannot be increased indefinitely. Unfortunately, a high-order $\Delta \Sigma$ TDC using SRO requires complex calibration to compensate for the error from frequency difference between the SROs. As a result, it consumes additional power and area as well as a long settling time [8].

In this paper, we propose a gated switched-ring oscillator (GSRO) which not only removes the need for complex calibration in high-order $\Delta \Sigma$ TDC but also allows for obtaining high OSR. Using the proposed GSRO, a novel second-order $\Delta \Sigma$ TDC is implemented, achieving low integrated noise and wide dynamic range with low complexity.

II. PROPOSED 1-1 MASH $\Delta \Sigma$ TDC USING GSRO

A 1-1 MASH TDC from [8] is shown in Fig. 1(a). The first stage SRO-TDC that performs first-order noise shaping is followed by a quantization error generator (QEGen) that produces a quantization error pulse. The first stage quantization error ($QE_1$) of width $T_{QE_1}$ is fed to the second stage SRO-TDC. Thus, it can be expected that this architecture will achieve second-order noise shaping. Unfortunately, there is frequency difference between the first and second stage oscillators during $T_{QE_1}$ as shown in Fig.1(b), since frequency change of the first stage SRO cannot be tracked by the second stage SRO. Hence, an undesired gain is multiplied to $QE_1$, which destroys the second-order noise shaping [8]. Although the frequency difference between the first and second stage oscillators can result from layout mismatch and manufacturing imperfections, frequency tracking error dominates the degradation of noise shaping. In [8], this problem is solved by using an off-chip calibration based on an LMS filter.

Fig. 1. Conventional implementation of the 1-1 MASH TDC using SRO. (a) Block diagram. (b) Timing diagram. $f_L$ represents the minimum frequency and $f_H$ represents the maximum frequency of the oscillator.

In this paper, we overcome this problem by proposing a GSRO whose operation principle is shown in Fig. 2. As can be seen, GSRO is basically an SRO with phase-holding gates added at supply and ground. Hence, GSRO acts as an SRO when the gates are closed and holds the phase like a GRO when the gates are open. Note that GSRO can also be con-

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considered as frequency controllable GRO. The schematic of the GSRO is shown in Fig. 4, which is basically a gated delay-line with frequency control via CTRL. Multi-path structure [4] is applied to reduce the gating skew error due to leakage current. The block diagram and timing diagram of the proposed TDC using GSRO are shown in Fig. 3. In the first stage, GSRO is configured as an SRO by closing the EN gates. In the second stage, QEGen shown in Fig. 5(a) generates quantization error pulse $QE_1$ and a frequency sync pulse $QE_{IN}$. An offset is added to $QE_1$ to avoid narrow pulse width which leads to a deadzone problem. The offset is easily subtracted in the digital cancellation filter (DCF). Since $QE_1$ controls the gates of the GSRO and $QE_{IN}$ controls the frequency of the GSRO, oscillation frequencies of the first stage SRO and second stage GSRO are the same during $T_{QE1}$, as shown in Fig. 3(b). Therefore, gain calibration is not needed and second-order noise shaping can be achieved by a simple DCF used in a typical MASH modulator as shown in Fig. 5(b).

Although the first stage SRO-TDC looks similar to the circuit shown in [5], there is a couple of key differences that are noteworthy. First, the first stage counter counts only one of the multi-phase outputs of the SRO instead of counting all the phases. As quantization error of the first stage is removed after the DCF, there is no need to minimize $T_{QE1}$ by counting all the phases. As a result, complexity and power consumption of the first stage SRO-TDC is significantly reduced. Second, the frequency of the SRO is designed to be higher than $f_S$ so that there exists at least one rising edge during a sampling period. This is because a residue pulse must be generated every cycle to complete the second-order noise-shaping. This is in contrast to [5] where the frequency of the SRO can be smaller than $f_S$ and hence a residue pulse may not be produced every cycle. Therefore, we employ a multi-bit counter shown in Fig. 6(a) to generate a residue pulse every cycle instead of a one-bit counter. One drawback of the multi-bit counter is that metastability may cause large error. In order to reduce the effect of meta-stability, a delayed clock generator (DCLKGen) is proposed by sampling the counter output ($CNT_{output}$) with a delayed clock as shown in Fig. 6(b) and (c).

Similar to MASH ADCs, some non-idealities of the proposed MASH TDC benefits from noise shaping. For example, $1/f$ noise, phase noise, and gating skew error of the second stage GSRO is reduced as they are first-order noise-shaped and filtered. In addition, the proposed structure is immune to mismatch between the delay-cells of the GSRO, since only the second stage uses multi-phase outputs and the effect of mismatch is second-order noise-shaped.

III. EXPERIMENTAL RESULTS

A prototype of the proposed $\Delta\Sigma$ TDC was fabricated in a 65nm CMOS and it occupies an active area of 250 x 210 $\mu$m$^2$ as shown in Fig. 7. The proposed TDC operates at 400 MS/s with 200 MHz input pulse rate. To verify the performance of the proposed TDC, power supply of an off-chip delay-line was modulated. The measured output spectrum of a 390 kHz, 19 ps peak-to-peak sinusoidal input with a time offset of approximately 1 ns is shown in Fig. 8, where it can
be seen that second-order noise-shaping is achieved with $1/f$ noise dominating at low frequencies. The measured integrated noise ($T_{int,rms}$) from 10 kHz to 4 MHz is -74.6 dB, which translates to 148 $f_{srms}$ at 200 MHz input pulse rate. The measured integrated noise for different OSRs is shown in Fig. 9, where the proposed TDC achieves better performance than a conventional SRO-TDC under the same OSR. Note that the integrated noise of the proposed TDC is limited by thermal and $1/f$ noise at higher OSRs (>100). The power consumption of the proposed TDC depends on the input pulse width, $T_{IN}$. The upper limit is 6.55 mW, which is when the input is always high. When the average input pulse width is 1 ns, the power consumption is 5.35 mW. The performance of the proposed TDC is summarized and compared with the recent state-of-the-art $\Delta \Sigma$ TDCs in Table I and Fig. 10. The proposed TDC achieves the widest bandwidth while achieving good FoM. Note that FoM1 used for $\Delta \Sigma$ converters is a better indication of the performance than FoM2 defined for Nyquist converters.

IV. CONCLUSION

In this paper, a novel all-digital second-order $\Delta \Sigma$ TDC has been proposed that achieves wide dynamic range, wide bandwidth and low integrated noise. Using the proposed GSRO, the order of noise-shaping has been increased by cascading GSRO-TDC without any calibration. Since time-resolution of the GSRO depends on the speed of logic gate, the proposed architecture is expected to gain higher performance with the continued scaling of the CMOS process.

V. ACKNOWLEDGMENTS

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* Does not include power and area consumed by off-chip calibration.
** Charge-pump with noise-shaping single slope quantizer.
*** FoM1 = DR + 10log_{10}(Bandwidth/Power) [dB], where DR = 20log_{10}(T_{range}/T_{int,rms}).
**** FoM2 = Power/2^{(DR−1.76)/6.02}/Bandwidth, where Bit = number of bit :

Fig. 9. Measured integrated noise for different OSRs. The integrated noise is varied by changing signal bandwidth.

Fig. 10. FoM comparison with recent reported ΔΣ TDCs.

REFERENCES