ABSTRACT
A novel five-transistor (5T) static memory cell is presented for applications in high-speed, low-power cache. The 5T design in 0.18µm bulk CMOS exhibits 57% faster operation speed, a 12% reduction in power, and a 6% reduction in area with respect to the standard 6T cell design.

I. INTRODUCTION
One of the most critical elements in systems such as microcontrollers, digital signal processors, and high-end CPU's is embedded cache. Bit-line leakage, interconnect capacitance, reduced supply voltage, and increased sub-threshold leakage have resulted in harsh operating environments. This work attacks these problems with a novel five-transistor (5T) cell that offers several attractive benefits as an alternative to previously published designs.

II. PREVIOUS DESIGNS
Several cell designs have been previously proposed as improvements to the standard six-transistor (6T) cell model. These include designs based on exploiting data statistics with asymmetric cells, the addition of leakage reduction circuitry, and the use of multiple threshold voltage transistors [1,2,3]. These methods generally require extra area overhead or special fabrication techniques.

Several cell structures shown in Fig. 1 have also been proposed as alternatives to the 6T design. Four-transistor (4T) cells suffer from reduced noise margins, unique fabrication requirements, and poor scalability. Similarly, seven-transistor (7T) cells exhibit small noise margins, added control complexity, and increased area [5]. Finally, it should be noted that a 5T cell shown in Fig. 1[b] has been published previously [6]. This design however, is only an incremental modification to the standard 6T cell and does not differ in its fundamental operation.

III. THE NEW FIVE-TRANSISTOR CELL
The memory cell proposed in this work is a new five-transistor (5T) design based on the 7T current-mode cell [5]. It requires fewer transistors than the standard 6T cell and at the same time, exhibits the same dynamic power improvements offered by the 7T cell. The proposed 5T cell is shown in Fig. 2. The inverter PFETS are connected directly to the bit-lines, and there is an additional transistor M5 coupling the inverters. Unlike standard cells, no word-line transistors are needed to provide access during the read and write cycles.

In equilibrium, M5 is off, data is preserved by the cross-coupled inverters, and no write signals are applied to the column NFETS. The bit-lines provide the supply voltage to the cells and are charged to Vdd through the PFETS at the top of the cell column.

During a read operation, only the access (AXS) signal of the selected cell is asserted to turn on M5. M5 is sized several times longer than minimum length to preserve data during an access. M5 in

![Figure 1 - Previous SRAM Cell Designs from (4), (6), (7), and (5) respectively.](image)
turn creates a current path from the bit-line to ground through the cell. The added current drawn from the PFETs at the top of the cell column creates a differential voltage on the bit-line pair sufficient for standard sense amplifiers.

Writing in the 5T cell also begins by asserting the AXS signal. At the same time, either Write1 or Write0 is activated to pull one of the bit-lines to approximately 2/3 Vdd. This reduces the current flowing through the cell and in turn, the voltage drop across M5. As a result, the cell NFET attached to the zero-node will turn on and the contents of the cell will flip to reflect the bit-line data. The read and write cycle are shown in Fig. 3.

IV. RESULTS AND CONCLUSIONS

Simulations were performed using extracted layouts of 5T and 6T cells in 1.8V, 0.18µm TSMC CMOS using Cadence Spectre and BSIM3v3 models. Transistor sizes for writing and pre-charging were optimized for the 5T and 6T cells independently. In addition, 100fF of bit-line capacitance and all extracted cell parasitics were included in the simulations. The 6T cell for comparison was designed according to the methodology in [7] but laid out under the same DRC constraints as the proposed 5T design, and optimized with a ß ratio of 1.39 and a cell ratio of 1.1 [7]. Given the results shown in Table 1, the 5T cell exhibits many advantages in a very straightforward, robust design. Reduced bit-line swinging minimizes power without compromising cell stability or speed. Such a design is suitable for many applications in systems with embedded cache and also in stand-alone IC’s.

Table 1 - Measured Performance Comparison

<table>
<thead>
<tr>
<th>Metric</th>
<th>New 5T Cell</th>
<th>6T Cell (DRC)</th>
<th>%Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Margin</td>
<td>~400mV</td>
<td>~250mV</td>
<td>+60%</td>
</tr>
<tr>
<td>Write Delay</td>
<td>469ps</td>
<td>1.1ns</td>
<td>-57%</td>
</tr>
<tr>
<td>Read Delay</td>
<td>300ps</td>
<td>120ps</td>
<td>+150%</td>
</tr>
<tr>
<td>Power</td>
<td>68.3µA</td>
<td>77.3µA</td>
<td>-12%</td>
</tr>
<tr>
<td>Area</td>
<td>(3.09x2.18)</td>
<td>(3.38x2.1)</td>
<td>-6%</td>
</tr>
</tbody>
</table>

V. REFERENCES