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Novel Reversible Multiplier Circuit in Nanotechnology

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Abstract: Reversible computation is of the growing interests to power minimization having applications in low power CMOS design, quantum computing, optical information processing, DNA computing, bioinformatics and nanotechnology. This paper proposes a novel 4x4 bit reversible Multiplier circuit. It is faster and has lower hardware complexity compared to the existing designs. In addition, the proposed reversible multiplier is better than the existing counterparts in term of number of gates and number of garbage outputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "MKG". The reversible MKG gate can work singly as a reversible full adder. In this paper we use MKG gates to construct the reversible multiplier circuit. The proposed reversible multiplier circuit can multiply two 4-bits binary numbers. It can be generalized for NxN bit multiplication.

Keywords: Reversible logic circuit . reversible multiplier . reversible logic gates . nanotechnology based systems

INTRODUCTION

An important factor in VLSI circuit design is power dissipation. R. Landauer's research in the early 1960s demonstrated that irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where $K = 1.3806505x10^{-23} m^2kg^{-2}K^{-1}$ (joules $Kelvin^{-1}$) is the Boltzmann's constant and T is the absolute temperature at which operation is performed [1]. Reversible logic circuits (or gates) are information lossless. Hence, reversible logic circuits have theoretically zero internal power dissipation. In 1973, Bennett proved that to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. A circuit is said to be reversible if the input vector can be uniquely determined from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs [4-6]. Thus, the number of inputs and outputs in reversible logic circuits (gates) are equal. Such circuits (gates) allow the reproduction of the inputs from observed outputs and we can recover the inputs from the outputs [3-5]. Reversible logic is a promising area of study with regard to the further technological advances. Reversible logic has received significant attention in recent years. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, quantum computing, thermodynamic technology, bioinformatics and nanotechnology. It is not possible to construct quantum circuits without reversible logic gates. Synthesis of reversible logic circuits is significantly more complicated than irreversible (conventional) logic circuits because in a reversible logic circuit, fan-out and feedback are not allowed [4].

A reversible circuit should have the following features [5]:

- Use minimum number of reversible logic gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

The output that is not used for further computations is called garbage output [6]. The input that is added to an nxk function to make it reversible is called constant input [7].

Addition and multiplication are two heavily used arithmetic operations in many computational units. It is necessary for the processors to have high speed multipliers. In this paper, a novel reversible multiplier circuit using reversible MKG gates and Peres gates is

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presented. We demonstrate that the proposed reversible multiplier is better than the existing counterparts in term of number of gates, number of garbage outputs and hardware complexity.

MATERIALS AND METHODS

Reversible logic: An n-input n-output function F is said to be reversible if there exists a one-to-one correspondence between the inputs and the outputs. Therefore, the input vector can be uniquely determined from the output vector.

Reversible logic gates: An nxn reversible logic gate can be represented as:

$$I_V = (I_1, I_2, I_3, \ldots, I_n)$$

$$O_V = (O_1, O_2, O_3, \ldots, O_n)$$

Where I_V and O_V are input and output vectors. In the past years, several reversible logic gates have been proposed. Some of them are: Feynman gate, FG [8], Toffoli gate, TG [9], Fredkin gate, FRG [10], Peres gate, PG [11], New Gate, NG [12], TSG gate, TSG [6] and MKG gate, MKG [13]. In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies.

Feynman gate (FG), also known as controlled-not gate (1-CNOT), is a 2x2 gate that can be described by the equations: P = B and Q = A⊕B, where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

Toffoli gate (TG), also known as controlled controlled-not (CCNOT), is a 3x3 gate. The Toffoli gate can be represented as:

$$I_V = (A, B, C)$$

$$O_V = (P = A, Q = B, R = AB \oplus C)$$

Where I_V and O_V are input and output vectors. The Toffoli gate is shown in Fig. 2.

Fredkin gate (FRG), also known as controlled permutation gate, is a 3x3 gate. It can be represented as:

$$I_V = (A, B, C)$$

$$O_V = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Where I_V and O_V are input and output vectors. It is shown in Fig. 3. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input is the same as the Hamming weight of its output.

Peres gate (PG), also known as New Toffoli Gate (NTG), combining Toffoli Gate and Feynman Gate is a 3x3 gate. It can be represented as:

$$I_v = (A, B, C)$$

$$O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$$

Where I_v and O_v are the input and output vectors. The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

New gate (NG), is a 3x3 gate. It can be represented as:

$$I_v = (A, B, C)$$

$$O_v = (P = A, Q = AB \oplus C, R = A'C' \oplus B')$$

Where I_v and O_v are the input and output vectors. The New gate is shown in Fig. 5.

TSG gate is a 4x4 reversible gate. The TSG gate is shown in Fig. 6, where each output is annotated with the corresponding logic expression.

MKG gate is a 4x4 reversible gate. The MKG gate can be represented as:

$$I_v = (A, B, C, D)$$

$$O_v = (P = A, Q = C, R = (A'D' \oplus B') \oplus C,$$

$$S = (A'D' \oplus B').C \oplus (AB \oplus D))$$

Where I_v and O_v are the input and output vectors. The MKG gate is shown in Fig. 7, where each output is annotated with the corresponding logic expression. The corresponding truth table of the MKG gate is depicted in Table 1. For more information about reversible logic gates see [13-16].

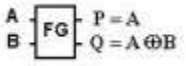


Fig. 1: Feynman gate

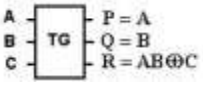


Fig. 2: Toffoli gate

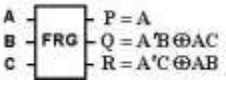


Fig. 3: Fredkin gate

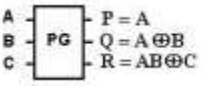


Fig. 4: Peres gate

Table 1: Truth table of proposed reversible MKG gate in [13]

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

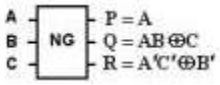


Fig. 5: New Gate (NG)

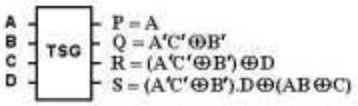


Fig. 6: TSG gate

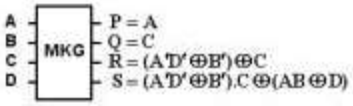


Fig. 7: Reversible MKG gate in [13]

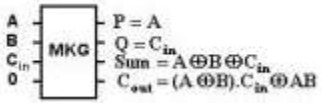


Fig. 8: Reversible MKG gate as a reversible full adder [13]

One of the prominent functionalities of the MKG gate is that it can work singly as a reversible full adder unit [13]. If I_v = (A, B, C_{in}, 0), then the output vector becomes: O_v = (P = A, Q = C_{in}, R = Sum, S = C_{out}). Therefore, we have both of the required outputs. Implementation of the MKG gate as the reversible full adder is shown in Fig. 8. The proposed reversible full adder circuit uses only one reversible logic gate. It produces only two garbage outputs. It requires only one constant input and it needs only one clock cycle to perform the operations [13]. It is proved that the proposed reversible full adder in [13] is better than the reversible full adder circuit in [6] in term of hardware complexity [13]. Let

			x_3	x_2	x_1	x_0	
			x	y_3	y_2	y_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig. 9: Partial products in a 4x4 multiplication

a = A two input EX-OR gate calculation
ß = A two input AND gate calculation
d = A NOT calculation
T = Total logical calculation

For [6]: T = 6a+3ß+3d and for [13]: T = 5a+3ß+3d. Thus, the proposed reversible full adder in [13] is better than the reversible full adder circuit in [6] in term of hardware complexity [13]. We use MKG gates to construct the novel reversible multiplier circuit.

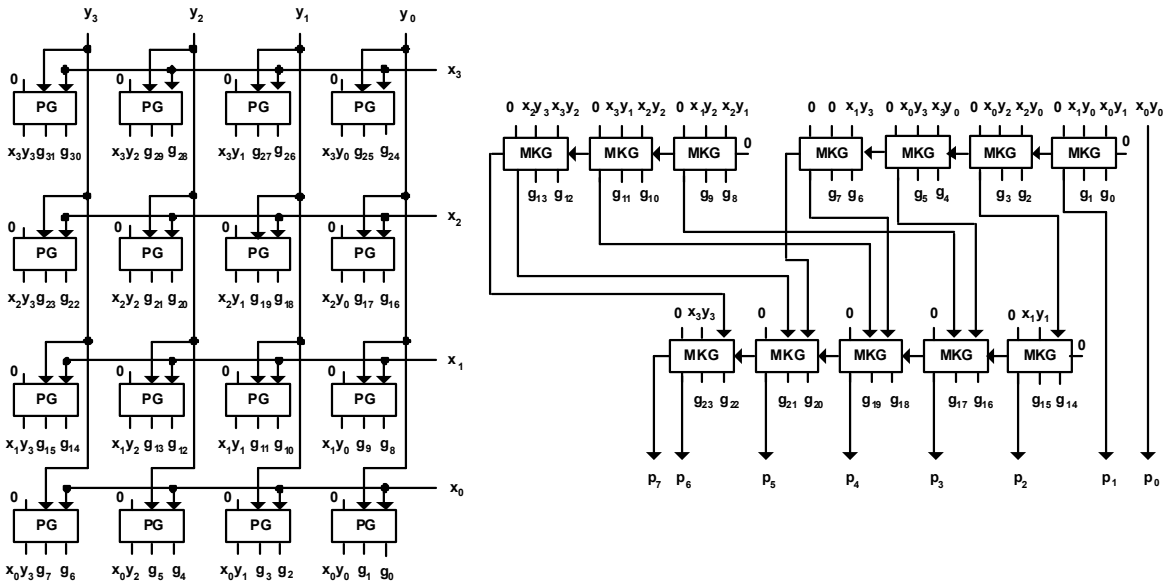
Novel Reversible Multiplier Circuit: Before the discussion of the proposed reversible 4x4 multiplier circuit, consider the partial products generation as shown in Fig. 9.

Our proposed reversible 4x4 multiplier circuit has two parts. First, the partial products are generated in parallel using Peres gates as shown in Fig. 10a. Then, the addition is performed as shown in Fig. 10b.

RESULTS AND DISCUSSION

Evaluation of the proposed reversible multiplier circuit: The proposed reversible multiplier circuit is more efficient than the existing circuits presented in [17, 18]. Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results in Table 2.

The only difference between partial products generation block in our design with the existing designs in [17, 18] is the use of Peres gates instead of Fredkin gates. It is because that the Perse gates have less logical calculation and less quantum cost than Fredkin gates. Thus, our proposed partial products generation block



(a). Proposed reversible partial products generation circuit using Peres gates

(b). Proposed reversible summation network using MKG gates

Fig. 10: Proposed 4x4 novel reversible multiplier circuit using MKG gates and Peres gates

Table 2: Comparative experimental results of different reversible multiplier circuits

	No. of gates	No. of garbage outputs	Total logical calculation
This study	16PG+12MKG=28	56	92a+52ß+36d
Existing Circuit [17]	16FRG+12NG+12TG=40	56	80a+100ß+68d
Existing Circuit [18]	16FRG+13TSG=29	58	110a+103ß+71d

has lower complexity and less quantum cost than the existing designs in [17, 18].

Comparing our proposed circuit with the existing circuits in [17, 18], it is found that the proposed design approach requires 28 reversible logic gates but the existing design in [17] requires 40 reversible gates and the existing design in [18] requires 29 reversible gates. So, the proposed circuit is better than [17, 18] in term of number of reversible logic gates, which is one of the main factors in reversible circuit design.

One of the main factors of a circuit is its hardware complexity. We can prove that our proposed circuit is also better than the existing approaches in term of hardware complexity. Let:

a = A two input EX-OR gate calculation
ß = A two input AND gate calculation
d = A NOT calculation

For [17] the Total logical calculation is: T = 80a+100ß+68d, for [18] the Total logical calculation is: T = 110a+103ß+71d and for our proposed reversible multiplier circuit, the Total logical calculation is: T = 92a+52ß+36d. Therefore, the proposed reversible multiplier circuit is better than the existing circuits in term of complexity.

Garbage output refers to the output of the reversible gate that is not used as a primary output or as input to other gates. One of the other major constraints in designing a reversible logic circuit is to lessen number of garbage outputs. Our proposed reversible multiplier circuit produces 56 garbage output, but the design in [18] produces 58 garbage outputs. So, we can state that our design approach is better than [18] in term of number of garbage outputs. It is to be noted that the design in [17] also produces 56 garbage outputs.

From the above discussion we can conclude that the propounded reversible multiplier circuit is better than the existing counterparts.

CONCLUSION

In this research, we presented a novel 4x4 bit reversible multiplier circuit using MKG gates and Peres gates. Table 2 illustrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of gates and number of garbage outputs.

Furthermore, the restrictions of reversible circuits were highly avoided. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology. All the proposed circuits are technology independent since quantum logic and optical logic implementations are not available.

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