DESIGN OF 320/321 PRESCALER CIRCUIT USING 4/5 PRESCALER

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Abstract: In this paper, Frequency divider by 2 circuit using D-flip-flop is done, based upon this a4/5 prescaler, 16/17 prescaler, 32/33 prescaler are verified. Along with it the design of wide band multimodulus 320/321 prescaler, CMOS single phase clock pre-scaler, wideband single phase clock 2/3 pre-scaler are also designed. A dynamic logic multimodulus flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 4/5 prescaler, 32/33 prescaler. Frequency synthesizer is implemented by using a phase-locked loop (PLL), and it is one of the power-hungry blocks in the RF front-end modules. The first stage of a frequency synthesizer is the frequency divider which consumes a large portion of power. The proposed multimodulus flexible divider provides a solution to the low power PLL synthesizers for various wireless communication devices.

KeyWords: Prescaler, PLL, Frequency Synthesizer

1. INTRODUCTION

The prescaler is the fundamental module for frequency synthesizers, it is also known as High speed divide-by-counter. As it operates at a higher frequency its design is crucial and it is the one which consumes more power than other blocks. A divide-by-counter consists of basic flip-flops, like D-flip-flop and extra logic gates, which determines the terminal count. Conventional prescaler circuits use current-mode logic (CML) latches [1] and suffer from the disadvantage of large load capacitance. This not only limits the maximum operating frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, D flip-flop based divide-by designs adopt dynamic logic flip-flops such as true-single-phase clock (TSPC) [2]–[4]. The designs can be further enhanced by using extended true-single-phase-clock (ETSPC) FFs for high speed and the designs can be further enhanced by using extended true-single-phase-clock (ETSPC) FFs for high speed and low power applications [5]–[10]. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra P-MOS/N-MOS transistor can form an integrated function of FF and AND/OR logic [7]. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design [8]. These two classic designs each contain 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a rationed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in [10] adopt a general TSPC logic family containing both rationed and ratio less inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario. In [11], a power gating technique by inserting an extra PMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations. Due to the quadratic dependency of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. In particular, here focus on low operations for power saving without sacrificing the speed performance. In this design, rationed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic.

In this paper, we start with basic divider by 2 circuit and enhance it to 4/5, 16/17, 32/33, 320/321 circuit design. After this, we design the basic CMOS single phase clock 2/3 prescaler circuit and wideband single phase clock 2/3 prescaler circuit.
1.1 DIVIDED by 2

Frequency divided by 2 circuit is done by using the basic D register. The circuit representation for the operation is as shown below figure 1.

![Figure 1: Divide by 2 circuit](image1)

Figure 2: timing waveform for Divide by 2 circuit

1.2 4 BY 5 PRESCALE

The 4by5 frequency prescaler circuit is done by using the basic D register and AND gate. The circuit representation for the operation is as shown below figure 3.

![Figure 3: 4by5 circuit](image2)

Figure 4: timing waveform for 4by5 circuit

1.3 16 BY 17 PRESCALER

The 16by17 frequency prescaler circuit is done by using the basic D register, AND gates, inverter. The circuit representation for the operation is as shown below figure 5.

![Figure 5: 16by17 prescaler circuit](image3)
1.4 32 BY 33 PRESCALER

The 32by33 frequency prescaler circuit is done by using the basic D register, AND gates. The circuit representation for the operation is as shown below figure 7.

1.5 320 BY 321 PRESCALER

The 320by321 frequency prescaler circuit is done by using the basic D register, AND gates. The circuit representation for the operation is as shown below figure 9.
2. SINGLE PHASE CLOCK circuits

The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the voltage-controlled oscillator. The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider. Much research has been focused on the prescaler design for its highest operating frequency. However, in the modern communication system, there is an increasing demand for multi-standards applications. A new wide-band high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology.

2.1 WIDEBAND SINGLE PHASE CLOCK 2/3 PRESCALER

The WIDEBAND SINGLE PHASE CLOCK 2/3 prescaler circuit is done by using the basic pMOS, nMOS transistors. The circuit representation for the operation is as shown below figure 11.

2.2 CMOS SINGLE PHASE CLOCK PRESCALER

The CMOS SINGLE PHASE CLOCK 2/3 prescaler circuit is done by using the basic pMOS, nMOS transistors along with gates and D register. The circuit representation for the operation is as shown below figure 13.
3. CONCLUSION

The design of a high-speed wide-band high resolution programmable frequency divider is investigated. A new reloadable D flip-flop for the high speed programmable frequency divider is proposed. This paper proposes a new frequency divider keeping the same function as a conventional one without employing a sallower counter to consume takes extra power and unnecessary chip area. The extended true single-phase clock (ETSPC) logic is proposed to increase the operating frequency. However, this causes additional power consumption. In modern wireless communication systems, the power consumption is a key consideration for the longer battery life. The MOS current mode logic (MCML) circuit, which is of high power consumption, is commonly used to achieve the high operating frequency, while a true single-phase clock (TSPC) dynamic circuit, which only consumes power during switching, has a lower operating frequency.

REFERENCES