Plasmonic interconnects versus conventional interconnects: a comparison of latency, cross-talk and energy costs

J.A. Conway[1]*, S. Sahni[2], and T. Szkopek[3]

[1]*The Aerospace Corporation,2350 E. El Segundo Blvd. El Segundo, CA 90245*
[2]*Department of Electrical Engineering, University of California, Los Angeles,420 Westwood Plaza, Los Angeles, CA 90095*
[3]*Department of Electrical and Computer Engineering, McGill University, 3480 University Street, Montréal, Québec, H3A 2A7*
josh.a.conway@aero.org,

Abstract: The continued scaling of integrated circuits will require advances in intra-chip interconnect technology to minimize delay, density of energy dissipation and cross-talk. We present the first quantitative comparison between the performance of metal wire interconnects, operated in the traditional manner by electric charge and discharge, versus the performance of metal wires operated as surface plasmon waveguides. Surface plasmon wire waveguides have the potential to reduce signal delay, but the high confinement required for low cross-talk amongst high density plasmon wire interconnects significantly increases energy dissipation per transmitted bit, above and beyond that required for electric charge/discharge interconnects at the same density.

OCIS codes: (200.4650) Optical Interconnects; (240.6680) Surface Plasmons; (250.3140) Integrated Optoelectronic Circuits.

References and links

1. "International Technology Roadmap for Semiconductors, 2005 Edition, Interconnect," http://www.itrs.net/Links/2005ITRS/Interconnect2005/Interconnect2005.pdf.
2. E. Ozbay, "Plasmonics: merging photonics and electronics at nanoscale dimensions," Science **311**, 189 (2006).
3. W. Steinhögl, G. Schindler, G. Steinlesberger, and M. Engelhardt., "Size-dependent resistivity of metallic wires in the mesoscopic range," Phys. Rev. B **66**, 075414 (2000).
4. W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt., "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," J. Appl. Phys. **97**, 023706 (2005).
5. G. E. Moore, "Cramming more components onto integrated circuits," Electronics **38**, 114 (1965).
6. D.A.B. Miller, "Optics for low-energy communication inside digital processors: quantum detectors, sources, and modulators as efficient impedance converters," Opt. Lett. **14**, 146, (1989).
7. K. Leosson , T. Nikolajsen, A. Boltasseva, and S. I. Bozhevolnyi , "Long-range surface plasmon polariton nanowire waveguides for device applications," Opt. Express, **14,** 314 (2006).
8. S.A. Backer, I. Suez, Z. Fresco, J.M.J. Frechet, J. Conway, S. Vedantam, H. Lee, and E. Yablonovitch, "Development of New Materials for Plasmonic Imaging Lithography at 476 nm," J. Vac. B (to be published).
9. L.G. Schulz, "The optical constants of silver, gold, copper, and aluminum. I. The absorption coefficient k," J. Opt. Soc. Am. **44**, 357 (1954).
10. L.G. Schulz and F. R. Tangherlini, "Optical constants of silver, gold, copper, and aluminum. II. The index of refraction n," J. Opt. Soc. Am. **44,** 362 (1954).
11. V.G. Padalka and I.N. Shklyarevskii, "Determination of the microcharacteristics of silver and gold from the infrared optical constants and the conductivity at 82 and 295deg K," Opt. Spectr. U.S.S.R. **11**, 527 (1961).
12. R. Philip and J. Trompette, "Simultaneous measurement of the optical constants and thickness of very thin silver films in the visible and near ultraviolet parts of the spectrum," Compt. Rend., **241**, 627 (1955).
13. J. Takahara, S. Yamagishi, H. Taki, A. Morimoto, and T. Kobayashi, "Guiding of a one-dimensional optical beam with nanometer diameter," Opt. Lett. **22**, 475 (1997).
14. D. F. P. Pile and D. K. Gramotnev, "Channel plasmon-polariton in a triangular groove on a metal surface," Opt. Lett. **29,** 1069–1071 (2004).

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

15. A. Hosseini, A. Nieuwoudt, and Y. Massoud, "Efficient Simulation of subwavelength plasmonic waveguides using implicitly restarted Arnoldi," Opt. Express, **14**, 7291 (2006).
16. T. Ono, M. Esashi, H. Yamada, Y. Sugawara, J. Takahara, and K. Hane, *Nano-Optics* (Springer, 2002), Chap. 5.
17. J.H. Chern, J. Huang, L. Arledge, P.C. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," IEEE Electron. Device Lett. **13**, 32 (1992).
18. "International Technology Roadmap for Semiconductors, 2005 Edition, Process Integration, Devices and Structures," http://www.itrs.net/Links/2005ITRS/PIDS2005.pdf.
19. M.I. Stockman, "Nanofocusing of Optical Energy in Tapered Plasmonic Waveguides," Phys. Rev. Lett., **93**, 137404 (2004).
20. J. Davis and J. Meindl, "Interconnect technology for gigascale integration," Kluwer (2003).

1. Introduction

As the scaling of integrated circuit components continues into the nanoelectronics era, the performance of metal wire interconnects is expected to degrade in a number of parameters. Most prominent are the increases in delay time for signal propagation, power dissipation and cross-talk amongst wires [1]. These problems arise from the fundamental physical limitations of transmitting information along metal wire interconnects by electric charging and discharging.

Concerns over signal delay, energy dissipation and cross-talk have caused some researchers in the semiconductor industry to consider alternatives to the charging and discharging of wires for communicating information across integrated circuits [1]. One such alternative is the use of optical surface-plasmons (SPs) propagating on metallic structures [2], such as metallic wires. SPs are charge density waves oscillating at optical frequencies on the surface of a metal, dressed with a highly localized electromagnetic field.

While it has been suggested that plasmons may present a solution to the "interconnect problem" of the integrated circuit industry, there has been no quantitative evaluation of plasmonic interconnects. In line with International Technology Roadmap for Semiconductors (ITRS) concerns [1], we specifically consider plasmonic waveguides for future intermediate-level interconnects. We present a comparison of the signal delay, energy dissipation per transmitted bit and cross-talk for interconnects based on conventional electric charging/discharging and the alternative of SP propagation.

We find that plasmonic interconnects offer reduced signal latency compared to conventional interconnects. However, the high SP confinement required for low cross-talk amongst high density plasmon wire interconnects significantly increases energy dissipation per transmitted bit, above and beyond that required for electric charge/discharge interconnects at the same density. Our findings provide quantitative information on the role that SPs might play in integrated circuit technology.

Our paper is organized as follows. Section 2 presents relevant background information on the physical limitations of conventional interconnects, and the alternative plasmonic interconnects that are considered in this paper. Sections 3, 4 and 5 describe the modeling techniques and results for interconnect signal delay, energy dissipation and cross-talk respectively. The implications of our work are discussed in a concluding Section 6.

2. Background

To appreciate the role that plasmonic interconnects may play in future integrated circuits, we review the physical limitations of conventional electric interconnects. The delay time for signal propagation is limited by an effective time constant typically dominated by the *RC* time of the interconnect itself (*R* and *C* being the total resistance and capacitance of the interconnect in question). As the cross-sectional area *A* of a metal wire is reduced, the wire resistance $R=\rho L/A$ increases (where ρ and *L* are wire resistivity and length, respectively). Furthermore, the effective resistivity ρ of the metal interconnect increases above the resistivity of bulk metal as the cross-sectional dimensions of the wire approach the mean free path of conduction electrons [3,4]. Since the distributed capacitance per unit length *c* does not change significantly as the interconnect is scaled down, the time for a signal to propagate across a

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

fixed distance of an integrated circuit will increase with geometric scaling, due to the undesirable increase in wire resistance.

The energy required to transmit a bit through a length of interconnect is a good measure of the energy efficiency of communication on an integrated circuit. The total energy required to charge a conventional wire of capacitance C through a potential change V is CV^2 (½ of this energy is the change in electrostatic potential energy of the wire, and ½ of this energy is dissipated in wire resistance during charging, barring slow adiabatic charging of the wire), leading to a dissipation of $\frac{1}{2}CV^2$ on average since only 50% of bit transmissions require a change in wire potential for an unbiased string of bits. One of the early motivations for circuit integration was the reduction of this energy consumption by reducing wire capacitance $C=cL$ between components through shorter inter-component distances [5]. The operating potential V is presently fixed to that required for switching of transistors (this choice of V is not optimal from a physical/information theoretic perspective, and the notion of impedance conversion to reduce V has already been proposed [6]). The distributed capacitance per unit length c of an interconnect is weakly dependent on geometry – and is in fact invariant upon geometric scaling of cross-sectional dimensions. It is only the ratio of cross-sectional dimensions that determines c, and not the absolute values of cross-sectional dimensions. Consequently, the energy dissipated per unit length per bit transmission is weakly dependent on interconnect scale. As interconnect density increases through scaling, the energy dissipated per unit of chip area will increase proportionally.

Finally, the increase in distributed wire resistance per unit length $r=R/L$ with geometric scaling increases the cross-talk amongst wires. As so-called aggressor wires are charged to transmit data, the potential on an adjacent victim wire will change substantially due to capacitive coupling $C_{wire\text{-}wire}$ between the aggressor and victim wires (see Fig. 1). At large operating frequencies typical of high-performance integrated circuits, the impedances between interconnects ($1/j\omega C_{wire\text{-}wire}$ where ω is the angular frequency) are reduced to values much lower than the resistance $R=rL$ through which current must flow in the victim wire to counteract induced potential changes. As a result, the scaling trends of increasing frequency and increasing wire resistance lead to greater cross-talk amongst wires. As cross-talk increases, bit-error-rates increase, so that interconnects themselves cease to be sufficiently reliable components in a fully operational integrated circuit.

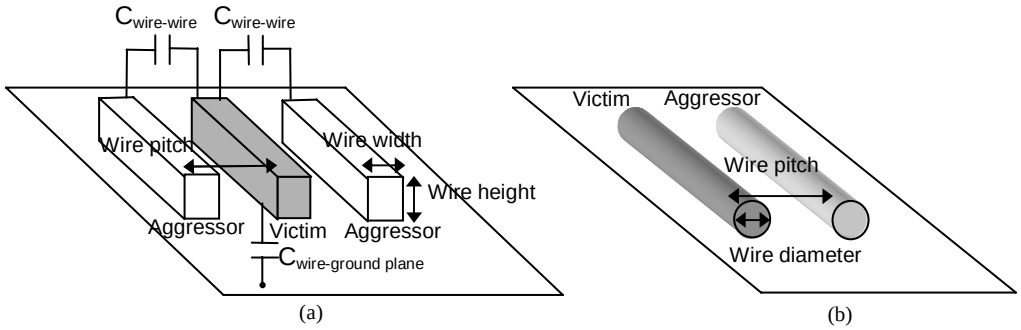

Fig. 1. (a) Electrostatic interconnect geometry where a victim wire's potential is changed as a result of capacitive coupling, $C_{wire\text{-}wire}$, to adjacent aggressor wires. (b) Geometry of adjacent cylindrical plasmonic waveguides where optical power couples from the aggressor into the victim.

The properties of SPs that make them worthy of consideration as an alternative means of communication in an integrated circuit are: (1) the group velocity of SPs can approach that of light, (2) SPs can be localized to the surface of a metal, so as to mitigate cross-talk, (3) the energy required to send and receive an SP pulse can be less than that needed for electric charging of a metallic wire, and (4) they have very large operating bandwidths. It is the highly localized nature of SPs that distinguishes them from optical modes in dielectric waveguides as a new means of integrated circuit communication.

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

As suggested by the ITRS [1], we specifically address plasmonic waveguides for future intermediate-level interconnects. The reason for this choice of interconnect level is clear. Local interconnects are too short to justify the addition of plasmonic sources and detectors. In addition to this, the reduction in length of local interconnects with standard scaling will mitigate most of the deleterious effects of reduced cross-sectional area. Global interconnects on the other hand, present plasmonic waveguides with strong competition from established technologies. Conventional high index contrast dielectric waveguides offer the same bandwidth and latency advantages of plasmonic waveguides. The long range plasmonic waveguides [7], which have propagation lengths suitable for global interconnects, tend to have transverse mode sizes akin to those of conventional dielectric waveguides. While it is possible that metallic waveguides may offer an advantage over dielectric waveguides if the materials systems are favorable to manufacturing, there is no substantial reduction in size associated with these modes. At the intermediate level however, the propagation lengths are short enough to employ plasmonic modes with cross-sectional areas significantly below the diffraction limit.

Since plasmonic circuits are a nascent area of research, it is our intent to analyze plasmonic interconnects under the best possible circumstances to establish an upper bound on performance expectations. Optimal choices of plasmonic materials and waveguide geometries have been made in this paper. Of the standard metals used for plasmonic wave-guiding (aluminum, gold, and silver), we have chosen to deal exclusively with silver because it has the lowest loss across the frequency spectrum of interest [8]. An optimistic estimate of interconnect performance is given by ignoring surface scattering effects and attributing bulk material optical constants to the plasmonic waveguide.

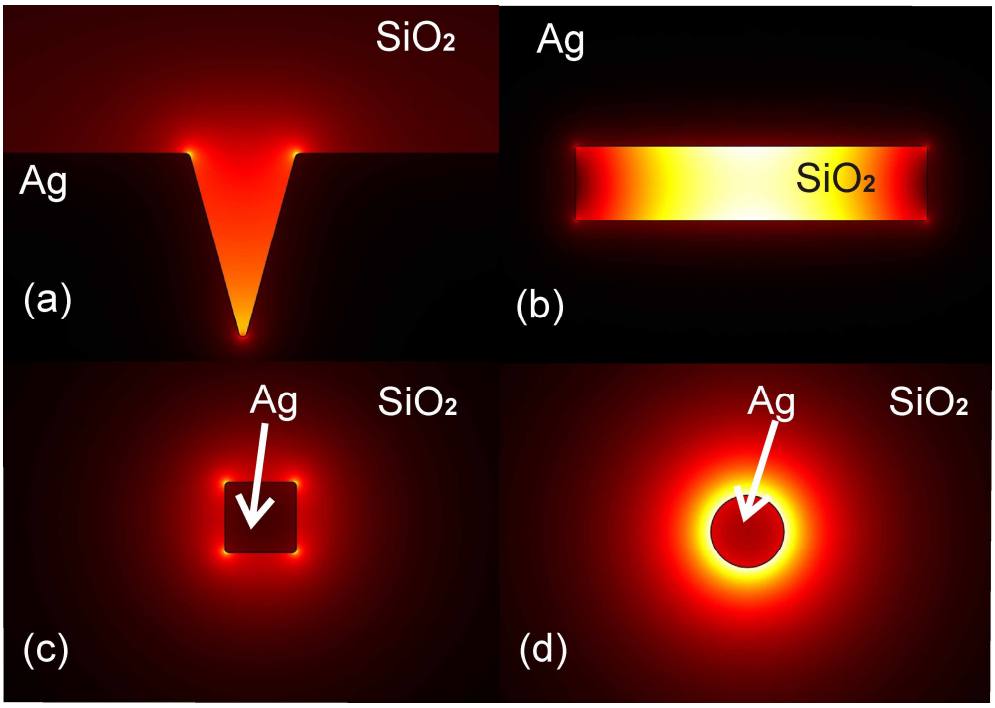

Fig. 2. Plot of the electric field magnitude superposed on cross-sections of various plasmonic waveguide geometries. (a) 55x100nm V-groove (b) 300x63.5nm SiO_2 strip in Ag (c) 47x47nm Ag square in SiO_2 and (d) 50nm diameter Ag cylinder in SiO_2. Each plot is normalized to the peak field. Note that the geometric scale varies between plots to best illustrate the field distribution.

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

We also wish to present the most favorable and physically relevant geometry. Figure 2 illustrates a cross-sectional plot of the electric field magnitude $E = (E_x^2 + E_y^2 + E_z^2)^{1/2}$ for various proposed plasmonic waveguides. All plots were generated using the commercially available software FEMLab ™ to solve for the eigenmodes in a silver/SiO_2 geometry with optical modes at a free-space wavelength of 850nm using empirically measured values for the dielectric constant of evaporated Ag [9-12]. All sharp corners have been rounded to a minimum radius of curvature of 2nm. Figures 2(c) and 2(d) illustrate a square (47x47nm) and circular [13] (50nm diameter) cross-section, respectively, of a silver waveguide in a matrix of SiO_2. Figures 2(a) and 2(b) illustrate a V-groove [14] (55x100nm) and a dielectric strip [15] (300x63.5nm) in a matrix of Ag. These dimensions were chosen such that each mode had an effective area (A_{eff}) equal to that of the 50nm diameter wire (approximately 14,500nm^2), defined by

$$A_{eff} = \frac{\left(\int |E|^2 dA\right)^2}{\int |E|^4 dA} \tag{1}$$

where the integral is taken over the entire cross-sectional plane.

Under these constraints, the dielectric strip geometry, followed closely by the V-groove had the greatest propagation lengths. These modes clearly have superior propagation characteristics on this length scale. Future intermediate interconnects, however, are predicted to have a wiring pitch below 50nm by 2016 [1]. Our simulations have not been able to find suitable dimensions of the dielectric strip or V-groove which will allow for this level of confinement in both the lateral and vertical dimensions. This is in accord with previous analysis of the cylindrical dielectric waveguide in a metallic matrix which showed a mode cut-off for diameters less than $0.3 \cdot 2\pi c_0/\omega$ [16] where c_0 is the speed of light in vacuum. The square and circular metallic waveguides surrounded by a dielectric, on the other hand, can be made to provide for adequate lateral and vertical mode confinement when their dimensions are reduced. The corners of the square waveguide create an enhancement of the field in that vicinity. The effect of these sharp features is to concentrate the optical energy, principally in the dielectric which yields an increased propagation length over the cylindrical waveguide. Our simulations, however, show that the square waveguide has only a slightly longer (<2%) propagation length. Since this difference is marginal and the cylindrical mode yields exact analytical solutions, it is the cylindrical mode that we will study.

3. Signal Delay

A graphic comparison of signal delay for plasmonic interconnects and conventional interconnects is given in Fig. 3. The signal delay of conventional interconnects is represented by the total $\tau = R_\Sigma C$ delay in Cu wires. The structure is taken to be similar to Fig. 1, namely a rectangular Cu interconnect in a low dielectric constant SiO_2 matrix, surrounded by other interconnects. The low dielectric constant material SiO_2 is chosen to provide an optimistic measure of performance. The interconnect width is parameterized to physically relevant values of 10nm and 50nm. Square electric interconnects have been considered as well as those with increased height:width aspect ratios (A/R) for reduced latency (A/R=2.0 and 1.7 for 10nm and 50 nm widths as respectively reported by ITRS [1]). The square electric interconnects provide a more direct physical comparison to circular cross-section SP waveguides. The distributed capacitances were calculated from empirical formulae [17], with a 3:1 ratio of interconnect pitch to width and a dielectric constant, ε_r, of 3.9. The total resistance $R = R_{wire} + R_{transistor}$ includes wire resistance $R_{wire} = \rho L/A$ and transistor access resistance $R_{transistor} = \rho'/W$, which we take here as that of a transistor of width W equal to interconnect width. The resistance constant ρ' is of the order of 100Ωμm and its exact value for different interconnect widths is again taken from ITRS data [18]. Empirically determined wire resistivity values were taken to be 3μΩcm, and 6μΩcm for wire widths of 50nm and 10nm respectively [3,4]. As expected, the delay increases dramatically with decreasing cross-sectional area. For a fixed cross-sectional geometry (ie. all cross-sectional lengths are scaled

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

by the same factor of 1/5), the distributed capacitances are constant and it is purely the resistance increase that leads to longer signal delays at reduced interconnect width.

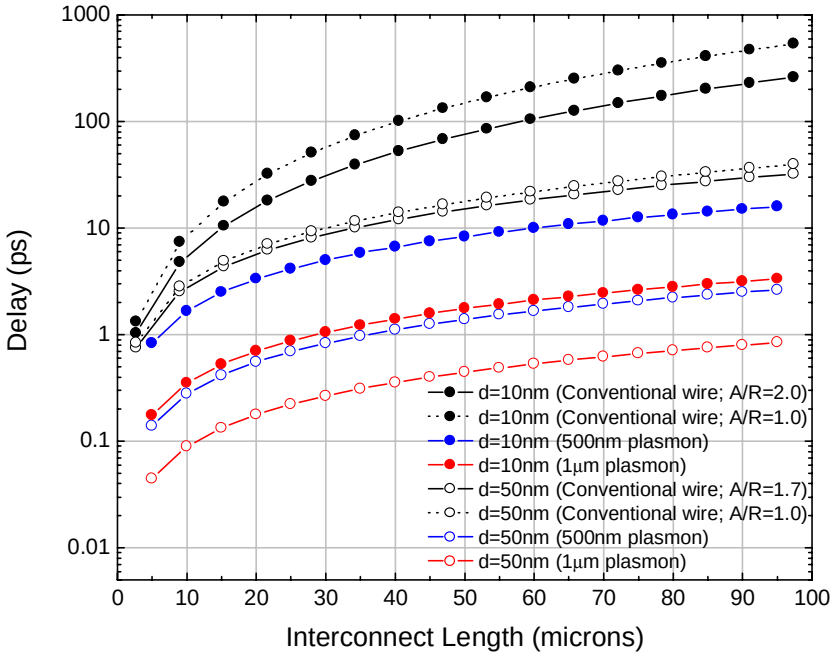

Fig. 3. The signal delay time for a Cu interconnect in an SiO_2 dielectric of width d and wire height:width aspect ratios of both 1.0 (square cross-section) and that reported by ITRS [1], surrounded with adjacent interconnects at a pitch:width ratio of 3:1. Also plotted is the signal delay for an isolated SP waveguide (a Ag cylinder of diameter d in SiO_2) at two different optical carrier frequencies (300THz, 600THz, or vacuum wavelengths 1μm and 500nm).

The signal delays estimated for plasmonic interconnects are also plotted in Fig. 3, and were calculated from numerically estimated group velocities of SPs propagating on cylindrical Ag wires in a SiO_2 matrix. The fundamental mode is TM and has the fortuitous property of achieving monotonically tighter confinement and reduced phase velocity as the wire radius is decreased [19]. Using the empirically determined optical constants of silver [9-12], the dispersion relation for SP propagation constant k as a function of SP angular frequency ω was solved numerically by finding the zeros of the dispersion equation [13],

$$\frac{\gamma_2 I_1(\gamma_1 a) K_0(\gamma_2 a)}{\gamma_1 I_0(\gamma_1 a) K_1(\gamma_2 a)} = -\frac{\varepsilon_2}{\varepsilon_1} \tag{2}$$

where a is wire radius, I_n and K_n are n^{th} order modified Bessel functions of the first and second kind, ε_2=2.25 is the exterior dielectric constant (of SiO_2), ε_1 is the frequency dependent dielectric constant of the Ag metal, and γ_1 (γ_2) are the evanescent field decay coefficients inside (outside) the metal wire satisfying the homogeneous dispersion relations,

$$\gamma_i = \left(k^2 - \varepsilon_i \frac{\omega^2}{c_0^{\,2}} \right)^{1/2} \tag{3}$$

The analytic results yield complex propagation constants in agreement with those found using the eigenmode solver of Section 2 to within 5 significant digits. Once the dispersion $\omega(k)$ was determined for 10nm diameter and 50nm diameter wires, group velocities ($\partial\omega/\partial k$) were calculated numerically. For a 10nm diameter wire, group velocities are $0.02c_0$, $0.10c_0$ at free space wavelengths of 500nm, 1μm; and for a 50nm diameter wire, group velocities are $0.12c_0$,

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

$0.38c_0$ at free space wavelengths of 500nm, 1μm. A free-space wavelength of 500nm has been chosen as representative of confined SP modes, with even shorter wavelengths resulting in unsuitably large loss (see Fig. 4). In contrast, a 1μm free space wavelength has been chosen as a representative of moderately confined modes, where the SP dispersion $\omega(k)$ approaches free space propagation. We do not consider longer free space wavelengths since the reduced SP confinement severely limits interconnect density, as described further in Section 5. Note that operating wavelengths of optical fiber networks are optimized to ~1550nm and ~1310nm to take advantage of the low loss window in silica fiber. However, a different set of physical constraints applies to the optimization of SP interconnects, for instance: Ohmic loss in metal is much more significant for SP modes on wires than absorption loss in silica.

Even the slowest SP mode considered (free space wavelength of 500nm on a 10nm wire) is found to result in less signal delay than 50nm wide conventional interconnects. In practice, the signal delay for the SPs would necessarily include the delay associated with emission of SPs onto the metal waveguides and detection of the SP's from metal waveguides. While this emitter/detector technology is not yet fully developed, it is clear that SP interconnects do have the potential to substantially reduce signal latency at high densities. We also point out that the energy of a photon with a free space wavelength of 500nm is well beyond the band edge of Si, this is in fact preferential because: 1) the SP would be confined to regions of either Ag or SiO_2, and hence would not be unintentionally absorbed by Si, and 2) the detection (and possibly emission) of SPs by Si based devices indeed requires an optical frequency beyond the Si band edge.

4. Energy Dissipated per Transmitted Bit

We now consider energy dissipation per bit of transmitted information. Conventional interconnects are driven directly by transistors at the operating voltages required for switching with sufficient signal to noise ratio at a prescribed bandwidth. The present operating voltage is of the order of 1V, which we take as representative of current practice [18]. The energy utilized per bit is on average $\langle E_E \rangle = \frac{1}{2}CV^2$, where C is the length dependent capacitance of the interconnect (transistor capacitance generally being negligible compared to that of intermediate interconnects).

We compare this energy cost directly with shot-noise limited transmission of SPs. The bit error rate (BER) for information transmission on an integrated circuit is roughly estimated to be 10^{-30}, based on transistor performance estimates of 1000 faults in 10^9 hours on a chip with 10^9 components operating at a clock rate of several 10^9 Hz [18]. Shot noise limited detection of an ideal coherent state with a mean of $\langle m \rangle$ plasmons for logical 1 and 0 plasmons for logical 0 results in a BER ideally equal to $\frac{1}{2}\exp(-\langle m \rangle)$. We therefore require a mean number $\frac{1}{2}\langle m \rangle = 34$ plasmons per bit in an unbiased channel to transmit information with a BER of 10^{-30}. Loss during transmission with an attenuation factor α requires that a minimum mean energy $\langle E_{SP} \rangle = \frac{1}{2}\hbar\omega\langle m \rangle \exp(\alpha L)$ be transmitted per bit, assuming unity quantum efficiency in emission and detection. The attenuation coefficient α, for the Ag wire geometry described above, was calculated from Eqs. (2,3) using the complex dielectric coefficients, including Ohmic losses in the metal. Graphically, α is represented as a decay length $L_0 = 1/\alpha$ in Fig. 4.

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

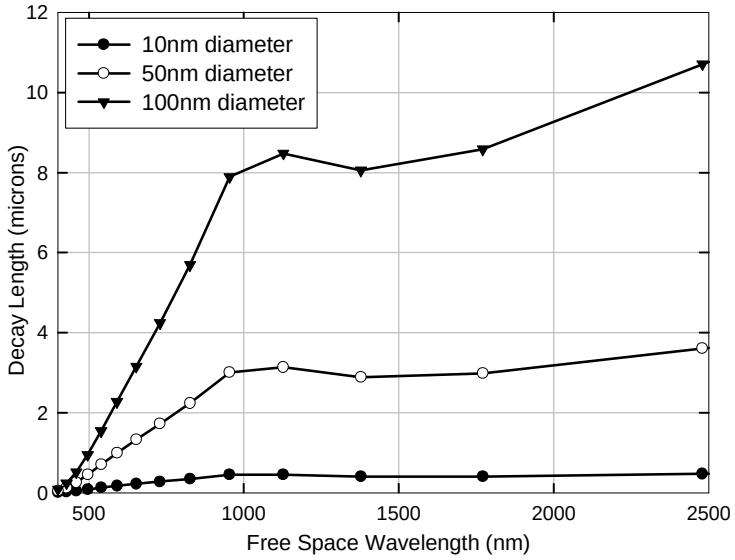

Fig. 4. Calculated attenuation lengths of SPs on Ag cylindrical wires of various diameters in a SiO_2 dielectric. The attenuation is weak at long wavelengths and large diameter wires, where SP confinement is weak and much of the SP energy lies in the relatively loss free dielectric.

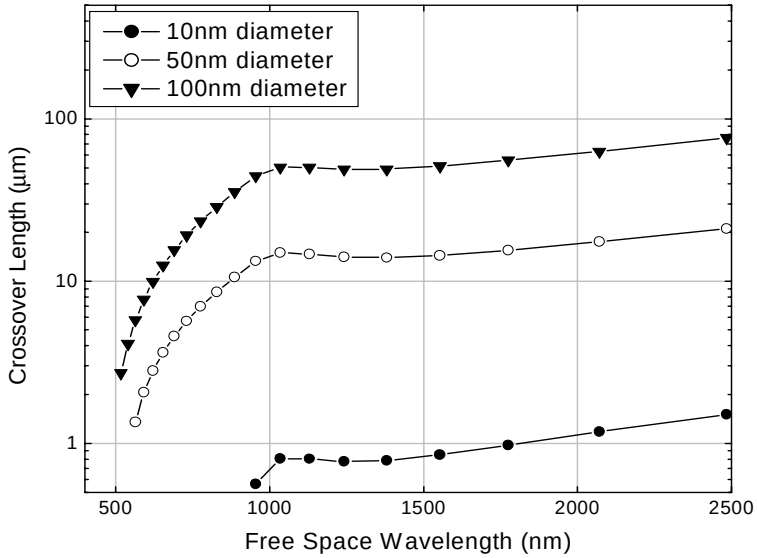

Fig. 5. Cross-over lengths beyond which it is more energy efficient to communicate via conventional electric interconnects rather than via SP interconnects due to attenuation of SPs. An operating voltage of 1V was assumed for electric interconnects of width *d*, unit aspect ratio and pitch:width ratio 3:1. The SP waveguides were assumed to be Ag cylinders of diameter *d* with no coupling to adjacent waveguides.

Note that the required energy per bit grows linearly for conventional interconnects, $\langle E_E \rangle = \frac{1}{2} c L V^2$, while energy per bit grows exponentially for SP interconnects, $\langle E_{SP} \rangle = \frac{1}{2} \hbar \omega \langle m \rangle \exp(\alpha L)$. Thus, there is a cross-over length beyond which conventional interconnects become more energy efficient per bit than plasmonic interconnects. We plot this cross-over length in Fig. 5 for conventional Cu interconnects of width *d* with unity aspect ratio and Ag SP waveguides of diameter *d* (i.e. the geometries described earlier). For the

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

purpose of comparison, we also include a previous generation of Cu interconnect, characterized by a 100nm width and 2μΩcm resistivity. It is clear that the plasmonic communication of information over distances of several microns using waveguides narrower than 50nm, or plasmon frequencies corresponding to free-space wavelengths less than 600nm is severely limited by energy efficiency concerns. We stress that this calculation only includes the effects of the plasmonic channel. When one incorporates plasmonic sources and detectors with finite quantum efficiency, the window of superior plasmonic efficiency will shrink further.

5. Cross-talk

Finally, we consider cross-talk between interconnects, or in other words, the leakage of signal energy from one interconnect to its neighbors. Cross-talk is typically quantified by a coupling length, corresponding to the length of victim wire (see Fig. 1(a)) required such that an aggressor will locally induce a voltage change on the victim equal to 25% of that required for a complete inversion of the logical value. The voltage transient on a victim wire subject to adjacent aggressor wires can be calculated from coupled line theory using distributed RC models for the interconnects [20]. The inductance of the wires can be ignored since the length scales are too short for it to be of significance. Assuming the same electric interconnect geometries described earlier, as illustrated in Fig. 1(a), the coupled differential equations that govern the transient voltages on the three wires can be written in matrix form as follows:

$$\frac{\partial^2}{\partial x^2}\begin{bmatrix} V_1(x,t) \\ V_2(x,t) \\ V_3(x,t) \end{bmatrix} = r \begin{bmatrix} \sum_{j=0,2,3} c_{1j} & -c_{12} & -c_{13} \\ -c_{21} & \sum_{j=0,1,3} c_{2j} & -c_{23} \\ -c_{31} & -c_{32} & \sum_{j=0,1,2} c_{3j} \end{bmatrix} \frac{\partial}{\partial t}\begin{bmatrix} V_1(x,t) \\ V_2(x,t) \\ V_3(x,t) \end{bmatrix} \quad (4)$$

where, $V_i(x,t)$ is the potential on the i^{th} wire at distance x and time t, r is the distributed resistance in each line, c_{ij} for $j \neq i$ and $j \neq 0$ is the distributed capacitance $C_{\text{wire-wire}}/L$ between the i^{th} and j^{th} wire and c_{ij} for $j = 0$ is the distributed capacitance $C_{\text{wire-groundplane}}/L$ of each wire to ground. Note that $\Sigma_j c_{ij}=c$ as defined in Section 2. The r and c_{ij} values were again calculated from standard empirical formulae [17]. The above equations can be decoupled and solved using a transformation derived from the eigenvectors of the capacitance matrix (the formulation is not reproduced here and can be found in [20]). The peak crosstalk voltage induced on the victim wire (wire 2) is estimated by assuming that the two aggressor wires (1 and 3) switch high simultaneously with identical rise times of 1ps. The 25% coupling lengths calculated for this case are plotted in Fig. 6.

It is clear that the coupling lengths are critically sensitive upon the capacitance between victim and aggressor. Achieving a given wire pitch with a reasonable cross-talk coupling length requires the physical wire width to be small, in conflict with the desire to minimize signal delay by increasing the cross-sectional area of interconnects. For example, packing interconnects to a pitch of 30nm will require the wire width to be of order 10 nm if a coupling length of order 10μm is to be attained, but this results in poor latency (see Fig. 3).

The coupling lengths expected for SPs guided on cylindrical metal wires are also plotted in Fig. 6. Confinement to metal surfaces is one of the key properties that have attracted interest in applying SPs to interconnect technology. SP waveguides will suffer from cross-talk due to evanescent field coupling amongst neighbors. We consider here, for simplicity, the rudimentary case of SP coupling between two adjacent waveguides (Fig. 1(b)), wherein energy is lost from one wire initially carrying an SP, to another wire initially without an SP. Since SPs are most likely to be detected through their energy rather than their field strength, it is appropriate to consider the 25% coupling length as that length at which 25% of the SP power has been transferred from one waveguide to the next. The 25% power coupling lengths were calculated from numerical simulations of SP propagation on two waveguides at various

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

wire pitches and diameters. A coupling coefficient κ quantifies evanescent field interaction: the spatial period of SP energy oscillation (neglecting loss) between coupled wires is $2\pi/\kappa$. This coupling coefficient was calculated from numerical simulations of the two wire system using commercial software (FEMLAB™) to execute finite element eigenmode solutions on a Lagrangian for the magnetic field. For various wire geometries and optical frequencies, the coupling coefficient was taken to be $\kappa=k_S-k_A$, where k_S is the wavevector of the symmetric "supermode" of the two wire system, and k_A is the wavevector of the antisymmetric "supermode". The 25% interaction lengths, $L_{25\%}=\pi/3\kappa$, are plotted in Fig. 6 as a function of wire pitch for representative diameters (10nm, 50nm) and optical frequencies (free space wavelengths of 500nm and 1μm).

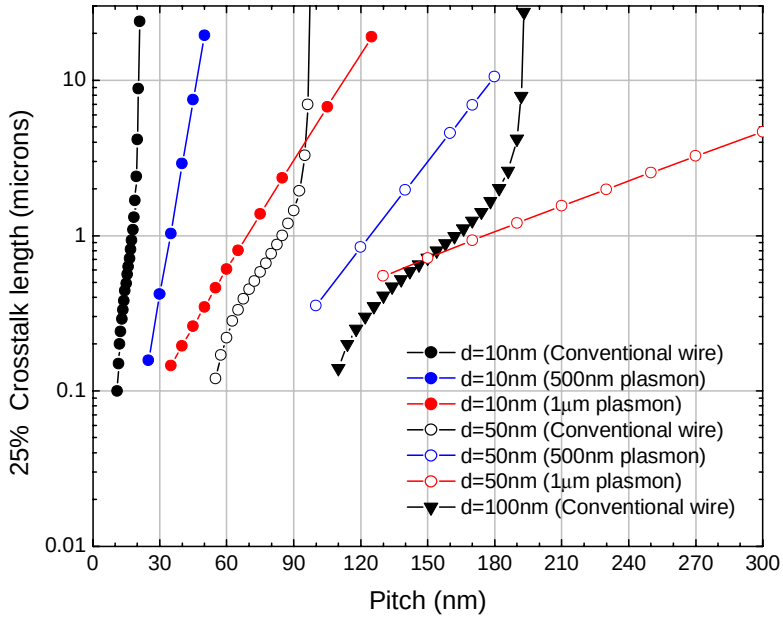

Fig. 6. The 25% coupling lengths for 1ps rise time pulses in electrostatic interconnect technology, plotted as a function of wire pitch for three fixed wire widths (10nm, 50nm, 100nm) and unit aspect ratio. Also shown are the 25% coupling lengths for SP interconnects for two fixed wire widths (10nm, 50nm) at two operating frequencies (300THz and 600THz, or vacuum wavelengths 1μm and 500nm).

For a given pitch, SP waveguides suffer from at least as much cross-talk as electric interconnects. It is only with reduced waveguide diameters or higher optical frequencies that SP waveguides may provide less crosstalk than conventional interconnects, and thus higher interconnect densities. As has already been pointed out, the tighter SP confinement of smaller diameter wires and/or higher optical frequencies corresponds to higher energy loss. A glance at Fig. 5 shows that the energy dissipated for bit transmission over several microns is already greater than conventional interconnects for wire diameters of 10nm or free space wavelengths of 500nm. SP waveguides can thus offer greater interconnect density only at the cost of increased energy dissipation per bit. Alternatively, a low interconnect density could be used to reduce energy dissipation per bit.

6. Conclusion

In summary, we have quantitatively shown that the notion of SP waveguides as interconnects has merit for the reduction of signal delay. Indeed, geometric scaling leading to an increased density of electric interconnects results in a severe penalty in delay, or the distance information can be communicated before cross-talk becomes significant. Conventional

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007

interconnects thus force a trade-off between signal delay and the interconnect density. In contrast, SP waveguide interconnects force a trade-off between energy per bit and interconnect density. Tightly confined SPs tend to be lossy, even in a low loss metal such as Ag, so that low cross-talk comes at the price of lossy propagation.

The efficiencies and footprints of future plasmonic sources and detectors are outside the scope of the present analysis, but these devices will degrade the effective energy per bit and latency performance of SP interconnects through finite device efficiencies (insertion loss) and device switching times. Our analysis provides an upper bound on the performance that can be expected from plasmonic interconnects. Note that SP waveguides have significantly higher bandwidth than conventional interconnects, but that this does not directly affect the energy per bit, crosstalk and latency although it could conceivably allow for multiplexing schemes like wavelength division multiplexing (WDM) to greatly enhance the capacity of a single wire. If such multiplexing were implemented, one could then use a larger and more efficient waveguide, such as those described in Section 2, which would greatly improve performance across all three parameters analyzed in this paper. Since such an add/drop architecture might require a footprint as large as the interconnect itself, and efficient devices have yet to be designed and demonstrated, the prospect of plasmonic WDM is significantly more speculative than the single channel waveguides described.

Although we have estimated most performance parameters of plasmonic waveguides within this paper, another parameter important to practical interconnect technology is long term reliability. The increasing current densities expected with the scaling of conventional electric wire interconnects, on the order of $J_{max}=10^6$-10^7 A/cm^2 [1], can result in significant electromigration causing permanent interconnect failure. Electromigration is the net transport of metal ions due to electron impact, and therefore no electromigration is expected to result from the zero time average current density of plasmons. However, the current density amplitude in a SP bearing wire may be comparable to the current density in an electric interconnect, as evidenced by the fact that Ohmic losses in an SP waveguide can exceed those of an electric interconnect (see Fig. 5). The long term effect of electron-ion collisions in SP wire waveguides has yet to be thoroughly investigated.

While surface plasmons are not an obvious replacement for intermediate electric interconnects, there is potential for use in other integrated circuit applications. For instance, there is a technological gap between conventional dielectric waveguides and the active region of an integrated circuit. Dielectric waveguides are well suited for transmitting information over long distances, but the fundamental limits on their size renders them impractical for communication below the highest (global) interconnect layer. However, SP waveguides, in the form of conventional tapered metallic vias for instance, could provide a means to transmit information from dielectric waveguides at the global interconnect level down to the transistor level, while employing materials used in conventional fabrication processes (copper and SiO_2).

Acknowledgements

A portion of this work was performed as part of The Aerospace Corporation's Independent Research and Development Program. We thank an anonymous reviewer for bringing to our attention the issue of electromigration.

#79038 - $15.00 USD Received 17 Jan 2007; revised 28 Mar 2007; accepted 28 Mar 2007; published 3 Apr 2007