Foundations and Practical Design of CMOS Image Sensors

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Area of the Tutorial: Sensory Systems

Keywords: CMOS Image Sensors, 3-D Image Capture, Signal Processing for CMOS Imagers, Data Conversion for CMOS Imagers, High Dynamic Range Sensors, Sensory-Processing Systems

Format of Tutorial: One Day

Instructor: Prof. Angel Rodriguez-Vázquez

Abstract

CMOS imagers are complex systems whose design requires quite different pieces of expertise, namely: pixels, analog signal processing, pixel readout and analog-to-digital conversion, digital signal processing, output drivers, etc. Confronting the design of new imagers require hence the concourse of multidisciplinary teams. However, because correct operation calls for the close interconnection among the different parts, global knowledge is mandatory for successful design. This is particularly pertinent for the newer generations of smart imagers required for high-end applications and/or requiring ultra high image capture, on-chip image correction, scene interpretation, high dynamic range capture, etc. All these features demand architectural and circuital innovations and pose significant challenges to designers. Also, the increased interest on sensors capable of capturing 3-D scenes raise new challenges at circuit level related to the necessity to interface pixels different from those employed for 2-D capture, on the one hand, and to extract and convert to digital domain time information, on the other hand.

This tutorial addresses the design of smart CMOS imagers by following a comprehensive and complete top-down approach where each subsystem is contemplated and described as a part of a whole. Starting the formulation of the performance metrics used to specify and characterize imagers, the tutorial explains how the subsystem behavior and non-idealities impact on the global imager metrics, thereby setting the basis to specify the subsystems for given global image sensor specs. Such methodology is illustrated in the tutorial via a dedicated, MATLAB-based modeling tool which will be employed to allow the attendees gaining insight on the impact of non-ideal sub-systems behaviors. The tutorial overviews the state-of-the-art regarding: pixels; analog signal processing and read-out circuitry; data conversion circuitry, covering both amplitude data converters (required for 2-D images) and time-to-digital converters (required for 3-D imagers); driving circuits. Practical design recipes are given for all these circuits. Architectures and circuit solutions employed for high dynamic range acquisition and embedded image processing are also reviewed. A case study is included where attendees are exposed to practical considerations to be taken during the design process, including the influence of packaging, optics and camera embedding.
Learning Objectives:

- To know the basic active pixel structures, including the challenges and non-idealities associated to their practical usage. Technological considerations for optimum performance will be outlined and proven macros will be shown. Pixels for 2-D and 3-D capture will be included as well as pixels with embedded memory for in-pixel CDS with global shuttering and the multi-functional pixels used for in-pixel spatial-temporal filtering, in pixel detection of salient points and early retina-like processing. Pixels employed for high dynamic range capture will also be overviewed. Pixel scaling will also be outlined.
- To know the architecture and the design implications of the analog readout channels employed for CMOS imagers, including strategies for error correction. As for pixels, non-idealities, their impact on overall imager performance and the ways to reduce this impact will be addressed seeking to provide attendees with the basic models and methods to design practical sensors.
- To know basic architectures and the design implications of the data converters employed for image sensors. Both conventional, amplitude-to-digital converters (used for 2-D capture) as well as time-to-digital converters (used for 3-D capture) will be covered. Architectures and design recipes for the most commonly employed architectures (pipeline, ramp, SAR, etc) will be given. Challenges created by the usage of per-column data converter architectures and the corresponding impact of fixed pattern noise will be introduced and illustrated by examples. Practical ways to overcome these problems (such as for instance data scrambling) will be presented. Closed loop techniques for error correction involving digital-to-analog feedback will be presented as well. Finally, architectures using adaptive quantization step for power reduction will be outlined.
- To know the operation, limitations and design procedures for driver circuits (LVDS).
- To know the architectures employed for embedded image processing through pixel processing, column processing and chip processing respectively. Examples of industrial sensors adopting these architectures will be presented and demonstrated in operation.
- The gain a global view of the architecture of a CMOS image sensor, the different sub-systems of this architecture (including circuits used for timing and biasing), the role and impact of these sub-systems, and the practical considerations to be taken into account when designing them in practice.
- To be exposed to a case study corresponding to the design of high-speed CMOS image sensor for machine inspection. To identify the different steps of a corresponding design flow and to illustrate either through behavioral simulation or through actual sensors the impact of the different design choices.

Target Audience:

The tutorial addresses fundamentals and practical considerations and provide a very detailed coverage of the state-of-the-art and the challenges of smart CMOS image sensors, including an extensive list of classified references. It is hence targeted for an ample audience, including:

- system engineers and practitioner,
- PhD students,
- university instructors

Pre-requisite is Master degree in Electrical Engineering with knowledge about electrical circuit design, MSFET operation and the basics of microelectronics.
**Description**

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This tutorial addresses the design of smart CMOS imagers by following a comprehensive and complete top-down approach where each subsystem is contemplated and described as a part of a whole. Starting the formulation of the performance metrics used to specify and characterize imagers, the tutorial explains how the subsystem behavior and non-idealities impact on the global imager metrics, thereby setting the basis to specify the subsystems for given global image sensor specs. Such methodology is illustrated in the tutorial via a dedicated, MATLAB-based modeling tool which will be employed to allow the attendees gaining insight on the impact of non-ideal sub-systems behaviors. The tutorial overviews the state-of-the-art regarding: pixels; analog signal processing and read-out circuitry; data conversion circuitry, covering both amplitude data converters (required for 2-D images) and time-to-digital converters (required for 3-D imagers); driving circuits. Practical design recipes are given for all these circuits. Architectures and circuit solutions employed for high dynamic range acquisition and embedded image processing are also reviewed. A case study is included where attendees are exposed to practical considerations to be taken during the design process, including the influence of packaging, optics and camera embedding.

This tutorial recast the knowledge acquired by Prof. Rodriguez-Vazquez in the course of his academic and industrial activities for more than 25 years. The company that he started is currently selling smart CMOS image sensors for different high-end asian markets. Modules contemplated in the tutorial inlude:

- System embedding and specification of CMOS image sensors. Implications of the system embedding on the design of the sensor.
- CMOS image sensor architectures. Identification, roles and challenges of the different sub-systems. Impact of the behavior of the subsystems onto the global sensor operation. Basic criteria for top-down specification mapping.
- CMOS active pixels, including: i) Pixels for 2-D capture; ii) Pixels for 3-D capture; iii) Pixels with embedded memory and/or processing; iv) Pixels for HDR capture; v) Multi-function pixels. Pixel coverage include:
  - Detailed study of pixel non-idealities as a function of timing and impact on the global sensor operation.
  - Formulation of pixel design equations.
  - Technological considerations and scaling.
- Read-out and data conversion circuitry. Covering both amplitude converters for 2-D capture and time converters for 3-D capture. Errors analysis and design equations.
- On-chip error correction and adaptive data conversion.
- Architectures for embedded image processing.
- Practical design considerations illustrated through a case study corresponding to an industrial design.
- Demonstrations through dedicated behavioral simulators and live demonstrators.
Instructor

Ángel Rodríguez-Vázquez received a PhD degree on Physics-Electronics in 1983. He is a Full Professor of Electronics at the University of Seville and the Institute of Microelectronics of Seville/CNM-CSIC. He is also the President and the responsible for long term R&D of Innovaciones Microelectrónicas S.L. (www.anafocus.com).

Prof. Rodríguez-Vázquez has always been looking for the balance between long term research and innovative industrial developments. He started a research unit on High-Performance Analog and Mixed-Signal VLSI Circuits of the Institute of Microelectronics of Seville/CNM-CSIC. He headed this unit until 2004, for more than 15 years, in the course of which he educated three generations of PhDs who are currently working at Academia and at Industry.

During these years, he conducted pioneering R&D activities on bio-inspired microelectronics, including vision chips and neuro-fuzzy interpolators and controllers. He was also a pioneer in the application of chaotic dynamics to instrumentation and communications; and his team completed the design and prototyping of the first, world-wide, integrated circuits with controllable chaotic behaviour and the design and prototyping of the first world-wide chaos-based communication MoDem chips. His team made also significant contributions to the area of structured analog and mixed-signal design and the area of data converter design, including the elaboration of advanced teaching materials on this topic for different industrial courses and the production of two widely quoted books on the design of high-performance CMOS sigma-delta converters.

Some 30 high-performance mixed-signal chips were successfully designed by his research unit at IMSE-CNM/CSIC until 2001 in the framework of different R&D programs and contracts. These include three generation of vision chips for high-speed applications, analog front-ends for XDSL MoDem, ADCs for wireless communications, ADCs for automotive sensors, chaotic signals generators, complete MoDem for power-line communications, etc. Many of these chips were state-of-the-art in their respective fields. Some of them entered in massive production. During this period of time he was also active regarding industrial training. He produced teaching materials on data converters that were employed by several companies. His courses got the Quality Label of EuroPractice.

He founded Innovaciones Microelectrónicas S.L. (AnaFocus) together with some colleagues in 2001. This company started operation after raising venture capital in January 2004. He served as the AnaFocus CEO until June 2009, a period in which the company grew from 2 employees until 50 employees and reached the threshold of maturity as a worldwide company specialized in the design and production of smart CMOS imagers and vision systems-on-chip. Since June 2009 he has been back to conduct long term research activities in the areas of vision systems using 3D integration technologies and medical electronics.

Prof. Rodríguez-Vázquez has authored/edited: 8 books; around 40 chapters in contributed books, including original tutorials on chaotic integrated circuits, design of data converters and design of chips for vision; and some 500 articles in peer-review specialized publications. He has presented many invited plenary lectures at different international conferences and has received a number of international awards for his research work (IEEE Guillemin-Cauer best paper award; the IEEE ECCTD best paper award and the IEEE ISCAS best demo-paper award) and was elected Fellow of the IEEE for his contributions to the design of chaos-based communication chips and neuro-fuzzy chips. His research work is widely quoted (some 4,500 quotes) and he has a h-index of 38.

Prof. Rodríguez-Vázquez has served and is currently serving as Editor, Associate Editor and Guest Editor for different IEEE and non-IEEE journals; he is in the committee of many international journals and conferences; and has chaired different international IEEE and SPIE conferences. Among others he has served as: TPC chair of IEEE ESSCIRC 1992 and 2010; General Chair of IEEE NDES 1996, IEEE CNNA 1996, IEEE ECCTD 2007 and IEEE ESSDERC-ESSCIRC 2010 and IEEE ICECS 2012. He served also as VP Region 8 of the IEEE Circuits and Systems Society (2009-2012) and as Chair of the IEEE CASS Fellow Evaluation Committee (2010, 2012 and 2013).