An Enhanced Slew Rate Output Capacitor-free Low Dropout Regulator Based on Differential Transconductance Amplifier

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ABSTRACT

A highly current-efficient and fast transient response capacitor-free low-dropout regulator (LDO) for System-on-Chip (SoC) applications is presented in this paper. The proposed architecture is implemented using 0.35 µm CMOS technology. The proposed circuit is based on differential transconductance and push-pull amplifier. Common mode feedback (CMFB) resistors and direct voltage spike detection using RC high pass filter are used to enhance the slew rate at the gate of the output transistor. Loop bandwidth is extended by adaptive biasing. This greatly improves the LDO transient response while preserving high current-efficiency. The output is regulated at 1.2 V with dropout voltage of 200 mV and a maximum load of 125 mA. Simulation results showed that the lowest consumed quiescent current is approximately 8 µA with a voltage spike and recovery time of less than 260 mV and 0.5 µs.

KEYWORDS

Low Dropout Regulator (LDO), Common-mode feedback (CMFB), Adaptive Biasing (ADB), High Pass Filter (HPF), Slew Rate

1 INTRODUCTION

Power management ICs (PMICs) for powering up different sub-circuit blocks integrated in SoC is a very promising approach in producing a more powerful and lighter advanced portable electronic gadgets [1]. Low dropout voltage regulators (LDOs) is one of the critical PMICs module in providing supply voltage to noise sensitive blocks such as digital, analog and RF blocks with high speed and precision [2], [3] as shown in Figure 1.

Conventional LDO requires external off-chip capacitor to overcome stability issue with high production cost [4]. However, SoC implementation is violated because it occupies large PCB area increasing the distance for power routing [2], [5].

For portable applications, current efficiency is a critical factor in prolonging the battery life of the devices by lowering down quiescent current $I_Q$ and dropout voltage $V_{DO}$ [3], [6]. However, there is a trade-off between efficiency and transient response. Recently, several techniques were proposed to improve the transient response of the LDO without degrading its current efficiency. In [6], class AB transconductance amplifier is used to improve the slew rate but it suffers from limited input common mode range and reduced GBW due to low and fixed $I_Q$. In [7], adaptive biasing (ADB) technique was adopted by increasing $I_Q$ proportionally to $I_{out}$ but it does not improve slew rate during voltage undershoot. Simpler method of detecting voltage transient by using RC high pass filter (HPF) was proposed by [8]. However, the LDO topology used is based on flipped voltage follower [9] which is known to have low loop gain, thus affecting the LDO regulating accuracy. In [10], slew rate is improved by a pair of common mode feedback (CMFB) resistors employed in transconductance amplifier adopted by [10]. Nevertheless, high loop gain is achieved by sacrificing stability due to increase in on-chip capacitance.

Here, a fast transient response yet current efficient LDO is presented in this paper.
2 PROPOSED ARCHITECTURE

The transient response of the LDO is determined by both loop bandwidth as well as slew rate at the gate of the output power transistors [3], [8], [10]. Therefore, by combining all the techniques discussed, the complete schematic of the proposed LDO architecture is shown in Figure 2. The reference voltage is set such that $V_{\text{ref}} = V_{\text{out}} = 1.2\,V$. The buffer serves as a driving circuit and to transfer the $V_{\text{ref}}$ the input of $G_m$ pair, $\sim V_{\text{ref}}$. The $G_m$ pair is made up by $M_L$, $M_8$, $M_{10}$ and $M_H$, $M_9$, $M_{11}$. Their function is to sense a differential voltage, $\Delta V = |\sim V_{\text{REF}} - V_{\text{out}}|$ to generate a differential output current as they work in complementary action.

If $V_{\text{out}}$ undershoots, $G_{mL}$ outputs a large amount of current momentarily while current is reduced at the output of $G_{mH}$. A pathway is created such that the gate capacitor of $M_{\text{pass}}$ can be quickly discharged via $M_{14}$ in the form of sinking current. Gate voltage of $M_{\text{pass}}$ is reduced and finally $V_{\text{out}}$ increases back to regulated value. Conversely, $V_{\text{out}}$ overshoots, $G_{mH}$ will output a large amount of current while current is reduced at the output of $G_{mL}$. Drain current in $M_{16}$ is momentarily increased by mirroring action by $M_{15}$ and $M_{17}$, providing a path to quickly charge up the gate capacitor of $M_{\text{pass}}$ in the form of sourcing current so that $V_{\text{out}}$ drops to regulated value.

When the LDO draws a large amount of $I_{\text{load}}$, limited quiescent current $I_Q$ causes the transient response to suffer. This is because the GBW is low. Thus, ADB circuit based on current mirror $M_{ab1}, M_{ab2}, M_{ab3}$ and $M_{ab4}$, the $I_Q$ is made directly proportional to the $I_{\text{load}}$ without degrading current efficiency improving transient response. The relationship between GBW and current is defined by

$$\text{GBW} = \frac{2G_m R_{FB} g_{m14,16}}{C_C} \propto \sqrt{I_Q + I_{AB}} \quad (1)$$

where $g_{m14,16}$ is the transconductance of transistors $M_{14}$ and $M_{16}$ respectively. Mathematically, $G_m$ can be represented by

$$G_{mH} = \beta_H \left( \Delta V + \frac{g_{m9}}{\beta_9} \right) \quad (2)$$

and

$$G_{mL} = \beta_L \left( -\Delta V + \frac{g_{m8}}{\beta_8} \right) \quad (3)$$

where $\beta$ corresponds to the transistor sizing in which

$$\beta = \mu C_{ox} \frac{W}{L} \quad (4)$$
2.1 Small Signal Analysis

The small signal model of the LDO is illustrated in Figure 3. $C_1$ and $C_2$ are lumped parasitic capacitance at node $V_L$ and $V_H$ contributed by $R_{FB}$, drain of $M_L, M_{12}, M_{H}, M_{13}$. The small signal transfer function, $A_v(s)$ is derived shown in (5) by assuming load capacitance $C_L > C_g, C_g, C_1, C_2$. $R_{out}$ is expected to be very small such that

$$R_{out} = R_{load}∥ R_{pass}∥ \frac{1}{g_m}∥ \frac{1}{g_{mp}}$$  \hspace{1cm} (6)

Then, $R_g$ is defined by:

$$R_g = R_{14}∥ R_{16}$$  \hspace{1cm} (7)

Dominant pole $p_{-3dB}$ and non-dominant poles $p_2$ and $p_3$ are defined respectively by

$$p_{-3dB} = -\frac{1}{R_g(C_g + g_{mp}R_{out}C_C)}$$  \hspace{1cm} (8)

$$p_2 = -\frac{1}{R_{FB}C_1} \frac{g_{mp}C_C}{(C_C+C_g)(C_L+C_C)}$$  \hspace{1cm} (9)

$$p_3 = -\frac{1}{R_{FB}C_1} \frac{g_{mp}C_C}{(C_C+C_g)(C_L+C_C)}$$  \hspace{1cm} (10)

A high DC gain can be achieved as defined by:

$$A_{dc} = 2G_m R_{FB} g_{m14,16} R_g g_{mp} R_{out}$$  \hspace{1cm} (11)

Since the phase margin is not constant and changes with load current, a minimum $C_C$ is required by setting minimum phase margin to 45°. This can be achieved by letting $p_2$ to be greater than GBW as shown:

$$p_2 > GBW$$  \hspace{1cm} (11)

Hence,

$$C_{C(min)} > 2C_1 R_{FB}^2 g_m g_{m14,16}$$  \hspace{1cm} (12)

2.2 Analysis of HPF RC components

According to [3], HPF network does not affect the DC biasing at steady state but it helps in injecting more transient current, $\Delta I_{M15}$ to improve the slew rate at the gate of $M_{pass}$. Figure 2 shows that coupling effect of $C_p$ causes the gate voltage of $M_{15}$ to increase momentarily when the output voltage overshoots. The increase in current can be found from [8]:

$$I_{M15} + \Delta I_{M15} = \beta M_{15}(V_{GS15} + \Delta V - V_{TH})^2 = \beta M_{15}[(V_{GS15} - V_{TH})^2 + \Delta V^2 + 2\Delta V(V_{GS15} - V_{TH})$$  \hspace{1cm} (13)

where

$$\Delta I_{M15} = \beta_1 \Delta V (\Delta V + V_{GS15} - V_{TH})$$  \hspace{1cm} (14)

From (11), in order to increase more transient current, the aspect ratio of $M_{15}, M_{16}$ and $M_{17}$ should be increased.

2.3 Analysis of CMFB Resistors

According to [10], slew rate can be enhanced if the slewing current $I_S = I_{M16} - I_{M14}$ is directly proportional to the nth order of differential voltage, $\Delta V^n$ at the input of $G_m$ pair. Circuit reported in [3] and [6] has only $n = 1$, but the proposed circuit has $n = 2$. By taking ADB into consideration,

$$I_S = 2\beta_{14,16} \beta_{H,L}^2 R_{FB} \Delta V \sqrt{\frac{2(l_{10,11} + I_{AB})}{\beta_{12,13} \beta_{R9}}} \frac{\Delta V + \sqrt{\frac{2(l_{10,11} + I_{AB})}{\beta_{R9}}}}{\sqrt{\frac{2(l_{10,11} + I_{AB})}{\beta_{R9}}}}$$  \hspace{1cm} (15)

where $I_{AB}$ is the adaptively biased current flowing through $M_{ab3}$ and $M_{ab4}$.
3 SIMULATION RESULTS & DISCUSSIONS

The proposed LDO is simulated to obtain its performance parameter. Simulation result shows that the total $I_Q$ is only 8.1 $\mu$A. Load transient is also done as shown in Figure 4 with the worst output capacitor of 100 pF realized by on-chip metal power lines and capacitive loads. LDO is able to settle in less than 460 $\mu$s from undershoot and 6 $\mu$s from overshoot with no more than 260 mV. However, settling time for $V_{out}$ undershoot and overshoot is different. This is because of the RC time constant for $M_{14}$ and $M_{16}$ is different. $M_{14}$ is responsible in sinking the current in which its time constant is shorter than $M_{16}$, which sources the current to charge up the gate of $M_{pass}$. This is due to larger parasitic capacitance contributed by $M_{16}$ as its size is relatively larger than $M_{14}$. Open loop response of the LDO is also simulated as shown in Figure 5. GBW of the LDO is extended when $I_Q$ increases proportionally to $I_{out}$, thus a faster transient response is achieved.

Performance comparison between the proposed LDO architecture and previous works is also done as shown in Table 1. A figure of merit ($FOM = \frac{t_s}{I_Q/I_{Load(max)}}$) proposed by [11] is adopted to measure the performance of the LDO in terms of transient response and current efficiency. A lower FOM indicates a better slewing performance.

<table>
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<th>Work</th>
<th>Year</th>
<th>Tech. (µm)</th>
<th>$V_{out}$ (V)</th>
<th>$I_{out}$ (mA)</th>
<th>$V_{DO}$ (mV)</th>
<th>$I_Q$ (µA)</th>
<th>$\Delta V_{out}$ (mV)</th>
<th>$t_s$ (µs)</th>
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4 CONCLUSION

The proposed LDO based on $G_M$ pair with HPF, adaptive biasing and CMFB resistors has been introduced. Based on the simulation results, the proposed LDO proves to be current efficient yet achieving fast transient response according to the figure of merit. Nevertheless, the proposed LDO still has to be laid-out in the future. If the post-layout simulation meets the requirements, the LDO will be fabricated for further testing.
5 REFERENCES


