A Digitally Controlled Linear Voltage Regulator in a 65nm CMOS Process

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Agenda

- Motivation
- Circuit Description
  - System Overview
  - Current Sensing
  - ADC
  - DAC
  - Digital Controller
- Stability Analysis
- Measurement Results
- Conclusion
Motivation

- Why Digital Control in an LDO?
  - Programmable Compensator Coefficients
    → Reuse of Design
  - Easy Portability of Design
  - Robustness of Digital Compensator
    → Process and Temperature Variation
  - Performance of Standard Analog LDOs Achievable
System Overview

- Control Loop
  - Pass Device - PMOS
  - Current Sensor
  - ADC
  - DAC
  - Digital Controller

- Protection
  - Over-Current Protection
  - Gate Over-Voltage Protection
Current Sensing

- 5 Current Comparators for Load Current Sensing
  - 4 Levels for Adjusting the Loopgain
  - 1 Level for Over Current Protection

- Adjusting the Controller Gain
  → Try to Compensate Load Dependency of Unity Gain Frequency
ADC

- Capacitive Flash Topology
  - Implicit Sample and Hold
  - Capacitive Voltage Divider
  - Interpolation
  - Window
  - 8MHz Sample Rate
  - 4 Bit

- 0.5 LSB Offset

- Nonlinear Transfer Curve
  - Fine Resolution Near Set Point
  - Coarse Resolution at Deviation from Set Point
**DAC**

- Charge Pump DAC
  - Current Output
  - Integrating Behavior for $V_{GS}$ of Pass Device
- 9 Bit Resolution + Sign Bit
- Digitally Programmable Gain ($I_{BIAS}$)
Digital Controller

- Digital PD Error Amplifier
- Clock: 8MHz
- Sync Clock: 8MHz with 9.6ns Time Advance
- “ADC Sample to DAC Out”-Delay: 28.8ns (3x 104MHz Clock Cycles)
- Protection Features: Over Current- and Gate Over Voltage Signal Will Decrease the $V_{GS}$ of the Pass Device
- Correction of Nonlinear ADC Transfer Curve (4 Bit $\rightarrow$ 7 Bit)

$$G_{PD}(z) = \frac{(k_p + k_D)}{z} \cdot z - k_D$$
Stability Analysis

- Model in MATLAB
- 5 Operating Ranges → 5 Sets of Controller Coefficients
- Unity Gain Frequency Almost Constant (~ 700kHz)
- Phase Margin > 55°
Measurement Results

- Transient Test Conditions:
  - Supply Voltage: 4V
  - Output Capacitor: 470nF
  - Load Current Step: 1mA ... 150mA / 1us

Static Performance:

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>3 V ... 5 V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>2.874 V</td>
</tr>
<tr>
<td>$I_{OUT-MAX}$</td>
<td>150 mA</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>470 nF</td>
</tr>
<tr>
<td>Quiescent Current ($I_{OUT} = 0$ mA)</td>
<td>188 uA</td>
</tr>
<tr>
<td>Static Load Regulation ($I_{OUT} = 150$ mA)</td>
<td>9 mV</td>
</tr>
<tr>
<td>Drop-Out Voltage</td>
<td>78 mV</td>
</tr>
<tr>
<td>LDO Active Area</td>
<td>0.152 mm²</td>
</tr>
</tbody>
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Measurement Screenshot:
Conclusion

- Fully Digitally Controlled LDO
  - Advantages of Digital Implementation
  - Competitive Performance to Analog Solutions

- Fast Transient Response

- Over-Current Protection

- Testchip in 65nm CMOS