Fast Locking and High Accurate Current Matching Phase-Locked Loop

Silin Liu and Yin Shi
Institute of Semiconductor, Chinese Academy of Sciences
Beijing, China
slliu@semi.ac.cn, yshi@red.semi.ac.cn

Abstract—In this paper, a charge-pump based phase-locked loop (CPLL) that can achieve fast locking and tiny deviation is proposed and analyzed. A lock-aid circuit is added to achieve fast locking of the CPLL. Besides, a novel differential charge pump which has good current matching characteristics and a PFD with delay cell has been used in this PLL. The proposed PLL circuit is designed based on the 0.35um 2P4M CMOS process with 3.3V/5V supply voltage. HSPICE simulation shows that the lock time of the proposed CPLL can be reduced by over 72% in comparison to the conventional PLL and its charge pump sink and source current mismatch is only 0.008%.

I. INTRODUCTION

CPLLS are widely used as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers, and disk drive electronics [1]-[3]. High-speed applications such as Dual Rate memory clock buffer, high-speed clock-and-data recovery and Quad Data Rate SRAM require CPLL to achieve fast locking. Some of the benefits of reduced lock time include increased uptime, reduced recovery times and power savings.

There are various solutions to reduce the lock time of a PLL [4]-[5], some of which involve increasing the bandwidth of the loop. But it is not always desirable or possible, especially when the bandwidth is already testing the limits of stability. The other relies on lock-aid circuits to achieve this goal. This paper describes and analyzes a fast locking CPLL with a novel lock aid technique.

Proper design of the charge pump (CP) is critical for high data rate and high accuracy in a CPLL. The current sources implementing the CP suffer from various nonidealities. In a MOS-based implementation, the current sources suffer from channel length modulation which leads to a CP current depending on the control voltage. Besides, there is a mismatch between PMOS and NMOS current sources in the CP causing pattern jitter. This mismatching can be reduced by the CP which is proposed in this paper.

II. PROPOSED ARCHITECTURE AND PRINCIPLE

A typical CPLL consists of a phase frequency detector (PFD), a CP, a passive loop filter (LF), a voltage controller oscillator (VCO), and a frequency divider, as shown in Fig.1. The CPLL lock process can be viewed as a two-stage process which includes frequency acquisition and phase acquisition. This distinction is important when trying to understand how to reduce the total lock time. The frequency acquisition of the lock process takes the majority of the time. This lock-aid circuit registers the frequency errors between the feedback and reference signals, and then supplies a fixed current $I_S$ to the VCO node that drives the loop towards frequency lock. Once frequency lock is detected, the lock-aid circuit shifts the part into the typical CPLL work mode. The fast-locking operation principle could be derived as follows.

![Figure 1: Block diagram of typical third-order CPLL](image1)
![Figure 2: Block diagram of the proposed fourth-order CPLL](image2)
The RC network representing the loop filter in Fig.1 can be described by two differential equations as shown below:

\[
\frac{dv_{\text{ctrl}}}{dt} = \frac{I_{\text{CP}}}{C_2} - \frac{v_{\text{ctrl}} - v_c}{RC_2} \quad (1)
\]

\[
\frac{dv_c}{dt} = \frac{v_{\text{ctrl}} - v_c}{RC_1} \quad (2)
\]

where \(v_{\text{ctrl}}\) represents the VCO control voltage and \(v_c\) represents the voltage across the primary loop filter capacitor \(C_1\). From equation (1) and (2), we can get

\[
\int_0^t dv_{\text{ctrl}} = \int_0^t \frac{I_{\text{CP}}}{C_2} \cdot \frac{v_{\text{ctrl}} - v_c}{RC_2} dt - \frac{C_1}{C_2} \int_0^t dv_c \quad (3)
\]

The loop filter in Fig.2 can be described as following:

\[
\frac{dv_{\text{ctrl}}}{dt} = \frac{I_{\text{CP}}}{C_2} - \frac{v_{\text{ctrl}} - v_c}{RC_2} \quad (4)
\]

\[
\frac{dv_c}{dt} = \frac{I_S}{C_1} + \frac{v_{\text{ctrl}} - v_c}{RC_1} \quad (5)
\]

Then the \(v_{\text{ctrl}}\) in Fig.2 is equal to

\[
\int_0^t dv_{\text{ctrl}} = (\frac{I_S}{C_2} + \frac{I_{\text{CP}}}{C_2}) \cdot v_c - \frac{C_1}{C_2} \int_0^t dv_c \quad (6)
\]

Compared to equations (3), we can get that the lock-aid circuit in Fig.2 can supply an extra current \(I_S\) to drives the VCO frequency toward the desired value, and the PFD locks the loop afterwards. The lock-aid circuit current \(I_S\) is much higher than the CP current \(I_{\text{CP}}\) and the lock-aid circuit can improve the locking time of this PLL.

III. CIRCUITS DESCRIPTION

A. Proposed Charge Pump

The CP topology is illustrated in Fig.3. The core component of the architecture is two symmetrical differential pairs that are fed from the bottom by two equivalent tail currents, respectively. Because the inputs stages are very symmetric and the two tail currents are generated by the same type of devices, a good current matching can be achieved. Besides, cascoded current mirrors whose layout is optimized to achieve high levels of device matching are used in the design, which helps to achieve a close match between the source and sink currents of the charge pump output.

A low transient time in the charge pump response is obtained by careful design of signal and device characteristics at the source nodes of \(M_1\), \(M_2\), \(M_4\) and \(M_5\). First, the parasitic capacitance at this node is minimized by using appropriate layout techniques to reduce the source capacitance of \(M_1\), \(M_2\), \(M_4\) and \(M_5\), the drain capacitance of \(M_3\) and \(M_6\), and the interconnect capacitance between each of the devices. Second, the voltage deviation is minimized at this node that occurs when \(UP\) or \(DOWN\) switches. The level converters depicted in Fig.3 accomplish this task by reducing the voltage variation at nodes \(\Phi_1\), \(\Phi_2\), \(\Phi_3\) and \(\Phi_4\) to less than 350mV and setting an appropriate dc bias.

B. PFD with Delay Cell

The PFD circuit used in this paper is composed of a tri-state PFD with delay cells, as shown in Fig.4. The PFD outputs two pairs of inverse signals \(UP\), \(UPN\), \(DOWN\) and \(DOWNN\) to control the CP. The delay cell circuit generates the clock delay to a fixed phase difference, which calibrates the time delay between output \(UP\) and \(UPN\) (or \(DOWN\) and \(DOWNN\)). This PFD has good linearity combines the proposed CP can achieve a good current matching without dead zone.
C. Frequency Comparator

For the implementation of the FC, a digital solution based on symmetric, cross-coupled counter was chosen, since this is a compact circuit that measures the frequency difference directly, making it most accurate when closest to the target frequency. This is an important differentiator from other frequency detection techniques. It eliminates any VCO-specific dependencies and effects. The solution chosen is based on what can be described as a symmetrical range controller. The range controller is implemented using two identical, synchronously resetable counters. The reference counter is clocked by the reference clock and asserts the pump up signal while the feedback counter is clocked by the feedback clock and asserts the pump down signal. As well as the pump signal, each counter outputs an “inhibit” signal and a “reset” signal. The inhibit signal is used by one counter to inhibit the other counter from outputting a pump signal while the reset signal is used to force the other counter into the zero state.

D. Loop Filter

The sources that generates control line ripple include current mismatch and pulse skew of the CP. Synchronized with the input reference clock, the ripple on the control line modulates the VCO frequency, resulting in clock jitter directly.

Consider a periodic ripple, $V_m \cos(\omega_{\text{ref}} t)$, imposed on a control voltage of a locked loop, as shown in Fig.5. The excessive phase caused by the ripple

$$\Delta \phi(t) = \int_0^t K_{VCO} V_m \cos \omega_{\text{ref}} \tau d\tau$$

$$= \frac{K_{VCO} V_m}{\omega_{\text{ref}}} \sin \omega_{\text{ref}} t$$

(7)

Noting that absolute jitter is defined as the deviation of the zero-crossing point of the output clock, we arrive at

$$\Delta T(t) = \frac{\Delta \phi(t)}{N \omega_{\text{ref}}} = \frac{K_{VCO} V_m}{N \omega_{\text{ref}}^2} \sin \omega_{\text{ref}} t$$

(8)

where $N$ denotes the divide ratio. The zero-crossing point waggles around the average point with a frequency of $\omega_{\text{ref}} / 2\pi$. For large divide ratio $N$, the rms jitter can be obtained as

$$(\Delta T)_{rms}^2 = \frac{\omega_{\text{ref}}}{2\pi} \int_0^{2\pi} \frac{K_{VCO}^2 V_m^2}{N^2 \omega_{\text{ref}}^2} \sin^2 \omega_{\text{ref}} t dt$$

(9)

It follows that

$$(\Delta T)_{rms} = \frac{K_{VCO} V_m}{\sqrt{2N} \omega_{\text{ref}}}$$

(10)

Since the excessive phase reaches a maximum at $t = (2k+1)\pi / (2\omega_{\text{ref}})$ where $k = 0, 1, 2, \ldots$, the peak-to-peak jitter can be calculated as

$$(\Delta T)_{pp} = \frac{2K_{VCO} V_m}{N \omega_{\text{ref}}^2}$$

(11)

Equations (10) and (11) reveal that the jitter caused by the
reference feedthrough is proportional to the ripple amplitude $V_m$. It discloses that higher-order loop filters reduce the control line disturbance. But higher-order loop filters are unstable most of the time. So as a trade-off, a two-order loop filter is used.

IV. SIMULATION AND TEST RESULTS

The proposed fast locking PLL with the lock-aid circuit has been designed and simulated based on the 0.35um 2P4M CMOS process with 3.3V/5V supply voltage. As depicted in Fig.6, x-axis represents the time scale and y-axis represents the controlled voltage of the PLL. The settling time (i.e. within 0.1% final frequency) of the proposed PLL and the conventional PLL are 959ns and nearly 8us, respectively. Thus, the locked time of the proposed PLL is reduced by over 72% in comparison with the conventional PLL.

Fig.7(a) shows that the current mismatching between the CP source current and sink current is no more than 75nA, which is only 0.008% of the CP current. As depicted in Fig.7 (b), the s axis represents the VCO control voltage ($V_{ctrl}$). The CP source current matches the sink current (i.e. within 3uA) in the range of $V_{ctrl}$ from 0.8V to 3.8V, which covers 60% of the VCO control voltage tuning range. The simulation results show that the proposed PLL has fast locking speed and good current matching. Table 1 summarizes the performance characteristic of the proposed PLL.

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<th>TABLE I. PERFORMANCE SUMMARY</th>
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<td>CP sink and source current absolute accuracy</td>
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<td>CP sink and source current mismatching</td>
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<td>Settling time</td>
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Fig.7. Simulation results for CP (a) Mismatching current of CP (b) CP current matching characteristics on VCO control node.

differential charge pump with level converters can achieve good current matching between the source and sink charge pump current and improve the PFD/CP linearity. The lock-aid circuit can reduce lock times in CPLL to less than 1us without reducing the bandwidth. The proposed PLL is especially important for the CPLL which have stringent lock time requirements and tiny deviation requirements.

REFERENCES


