

RESEARCH ARTICLE

# A Novel Picosecond Pulse Generation Circuit Based on SRD and NLTL

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## Abstract

Because of the importance of ultra-wideband (UWB) radar in various applications, short pulse generation in UWB systems has attracted a lot of attention in recent years. In order to shorten the pulse, nonlinear transmission line (NLTL) is imported, which expands the application of step recovery diode (SRD) for pulse generation. Detailed analysis and equations for this SRD and NLTL-based pulse generation are provided and verified by simulation and experimental results. Factors that could cause pulse waveform distortions are also analyzed. The generator circuit presented in this paper generates 130ps and 3.3V pulse, which can be used in UWB radar systems that require sub-nanosecond pulses.



## OPEN ACCESS

**Citation:** Zhou J, Lu Q, Liu F, Li Y (2016) A Novel Picosecond Pulse Generation Circuit Based on SRD and NLTL. PLoS ONE 11(2): e0149645. doi:10.1371/journal.pone.0149645

**Editor:** Maria Rosaria Scarfi, National Research Council, ITALY

**Received:** August 8, 2015

**Accepted:** February 3, 2016

**Published:** February 26, 2016

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**Data Availability Statement:** All relevant data are within the paper.

**Funding:** This project is supported by the Chinese Defense Advance Research Program of Science and Technology, China (Grant No. 40404110203). The funders had no role in study design, data collection and analysis, decision to publish, or preparation of the manuscript.

**Competing Interests:** The authors have declared that no competing interests exist.

## Introduction

Nowadays, UWB radars are finding many applications in the areas of medical imaging, non-destructive testing, subsurface identifying, distance measuring, automobile traffic control and security systems [1–6], by transmitting high-intensity pulses and analyzing the reflection signals. Initially, the frequency spectrum of the UWB radar signals can be extended from low frequency to ultra-high frequency, so that it is highly penetrating and has great resolution. Furthermore, the UWB radar has low spectral density and is quite interference-proof, which is very helpful in short-range transmission. Therefore, this radar technology has attracted a lot of researchers and concerned industries across the globe to use it in any and every way for academic, business, and research purposes since the Federal Communications Commission (FCC) made the use of UWB license-free in 2002 [7].

To achieve a reliable sensing performance, however, it is necessary to develop a pulse generator with sufficient peak power and the shortest possible rise-time. Various approaches have been proposed for the design of a pulse generator for radar sensor application. CMOS integrated circuits-based pulse generators are developed to attain flexibility in controlling the pulse shape [8, 9]. However, this method has a long development time and high design cost because some of the components are customized. Other off-the-shelf designs include avalanche transistors [10], tunnel diodes [11], nonlinear transmission lines (NLTLs) [12], photoconductive switches [13], bipolar transistors [14], field effect transistors (FETs) [15], and SRDs [16–24].

Wang *et al.* [10] reported that an ultra-wideband nanosecond pulse was designed based on the avalanche effect of the avalanche transistor, where the pulse full width is 890ps and pulse

amplitude is -11.2V. However, the maximum pulse repetition frequency by this method is limited, and the transistor lifetime is short. In Ruai and Konishi's study [11], a resonant tunnel diode was utilized to produce very short pulses for switching and harmonic generation applications, but the output pulse amplitude was limited, generally speaking, not greater than 1V. Among the off-the-shelf designs, the SRD has been used as a key device because it can be easy to fabricate, cost-effective and capable of generating pulses with sharp transition edge. With the progress in electronics, the width of the narrow pulses generated via SRD is limited and cannot meet further requirements on bandwidth due to the constraints on transit time and the carrier's lifetime. Later on, NLTL was introduced to the narrow pulse circuit.

This paper proposes a method which can generate picosecond pulses by using both SRD and NLTL. SRD is the key narrow pulse-generating component used to generate 220ps narrow bands and then NLTL is used to further narrow the width to 130ps, with the amplitude being 3.3V.

The rest of the paper is organized as follows: Section II presents the pulse generator circuit design, which consists of SRD structure, circuit generating and simulation. Section III discusses the principle of NLTL. In Section IV, we discuss our experimentation/evaluation procedure and analyze the results achieved. Section V finally concludes the paper.

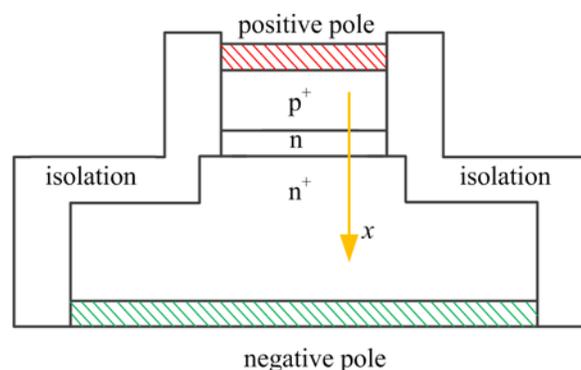
## Circuit Design

### 2.1 SRD structure

SRD is a PN junction diode whose impurity is distributed unusually, as shown in Fig 1. Between the high doping  $P^+$  layer and the high doping  $N^+$  layer is a low doping N-type layer. It is a typical slowly varying junction structure. When SRD converts from forward exciting voltage to negative exciting voltage, a strong backward current flows continuously until it terminates at a time instant, forming a steep step voltage. The narrow pulse can be generated in this way.

The principles for this phenomenon are as follows:

1. When SRD is in the positive bias, both sides of the PN junction are infused with many minority carriers. The special impurity distribution in SRD facilitates the increase in the injected minority carriers, and creates the retarding fields at both sides of the junction which can impede the proliferation of minority carriers, thus concentrating a large number of minority carriers in the narrow regions near the junction. Furthermore, the lifetime of the minority carriers is so long that they cannot be recombinant during the period of positive bias.



**Fig 1. Impurity profile of general SRD.**

doi:10.1371/journal.pone.0149645.g001

- When the positive bias converts to the negative bias, these stored minority carriers will flow in the direction opposite to the injection, forming a strong backward current. When all minority carriers are extracted, the backward current will be reduced to an extremely low level suddenly, cutting off the diode and forming the step voltage.

### 2.2 Pulse-generating circuit

The SRD pulse-generating circuit is shown in Fig 2(A). SRD can be treated equivalently as a small resistance and a large capacitance when the forward direction is conducting and its on-state voltage is about 0.5V. The on-state equivalent circuit is shown in Fig 2(B). In the case of the SRD conversion from the forward to the backward bias, SRD is still on at a voltage of about 0.3V and the current is in the reverse direction before the SRD junction charge is depleted. Furthermore, SRD can be equivalently seen as a variable capacitance at reverse cut-off, and the equivalent circuit is shown in Fig 2(C).

The time domain response of the circuit since the instance of the SRD cut-off will be analyzed as follows. To facilitate analysis, consider that the capacitance value  $C_d$  is constant. The voltages at both sides of SRD are the on-state voltages, when SRD is on and stable. In Fig 2(C), according to the Kirchhoff theorem, we have:

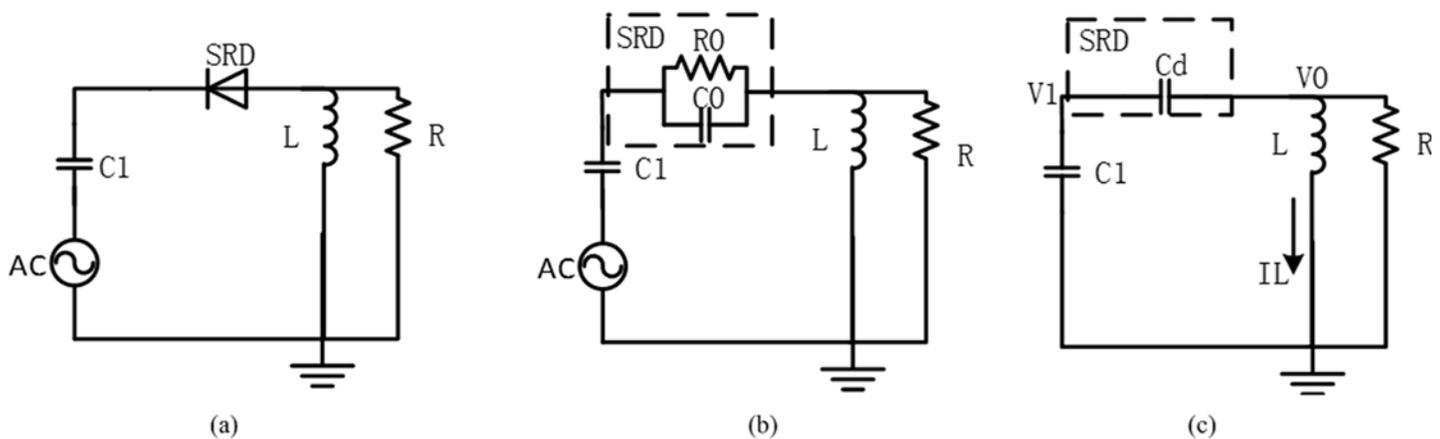
$$C_1 \frac{dV_1}{dt} + I_L + \frac{V_0}{R} = 0 \tag{1}$$

$$L \frac{dI_L}{dt} = V_0 \tag{2}$$

$$C_1 \frac{dV_1}{dt} = C_d \frac{d(V_0 - V_1)}{dt} \tag{3}$$

Eliminating  $V_1$  and  $I_L$  in the above equation yields the third-order differential equation of the voltage  $V_0$  at both sides of SRD:

$$\frac{C_1 C_d}{C_1 + C_d} \frac{d^2 V_0}{dt^2} + \frac{dV_0}{R dt} + \frac{V_0}{L} = 0 \tag{4}$$



**Fig 2. Pulse producing circuit based on SRD and equivalent circuit.** (a) Principle chart (b) Equivalent circuit during conduction (c) Equivalent circuit during cut-off.

doi:10.1371/journal.pone.0149645.g002

Consider that the values of  $V_0$ ,  $V_1$  and  $I_L$  at the time instance of zero are equal to  $V_{0(0)}$ ,  $V_{1(0)}$ , and  $I_{L(0)}$ , respectively, then the boundary condition in Eq 4 is:

$$\begin{cases} V_0(0) = V_{0(0)} \\ \frac{dV_0(0)}{dt} = -\frac{C_1 + C_d}{C_1 C_d} \left( I_L(0) + \frac{V_0(0)}{R} \right) \end{cases} \quad (5)$$

According to the infinitesimal analysis principles,  $V_0$  can be computed using Eq 4 and Eq 5 when the values of  $C_d$ ,  $L$ ,  $C_1$  and  $R$  are known as Eq 6:

$$\begin{aligned} V_0(t) = & \frac{-\frac{C_1 + C_d}{C_1 C_d} \left( I_L(0) + \frac{V_0(0)}{R} \right) - V_0(0)x_2}{x_1 - x_2} e^{x_1 t} \\ & + \frac{-\frac{C_1 + C_d}{C_1 C_d} \left( I_L(0) + \frac{V_0(0)}{R} \right) - V_0(0)x_1}{x_2 - x_1} e^{x_2 t} \end{aligned} \quad (6)$$

Where  $x_1 = \frac{\frac{C_1 + C_d}{C_1 C_d R} + \sqrt{\frac{(C_1 + C_d)^2}{(C_1 C_d R)^2} - \frac{4(C_1 + C_d)}{C_1 C_d L}}}{2}$ ,  $x_2 = \frac{\frac{C_1 + C_d}{C_1 C_d R} - \sqrt{\frac{(C_1 + C_d)^2}{(C_1 C_d R)^2} - \frac{4(C_1 + C_d)}{C_1 C_d L}}}{2}$

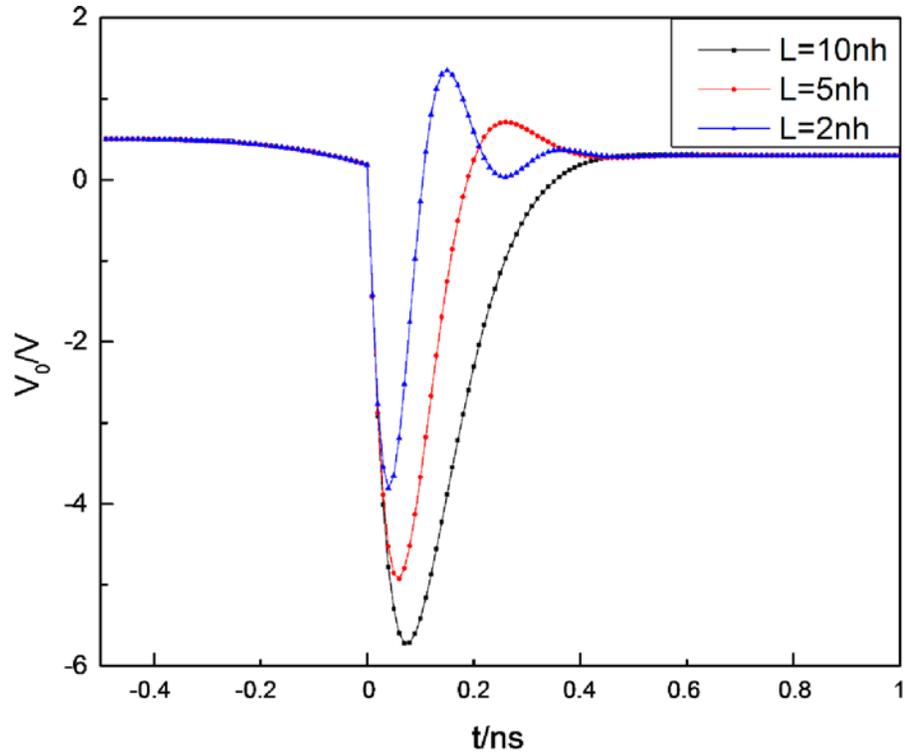
### 2.3 Circuit simulation

In order to analyze the influence of  $C_d$ ,  $L$ ,  $C_1$  and  $R$  on the  $V_0$ , we design simulations in Matlab, as shown in Fig 3.

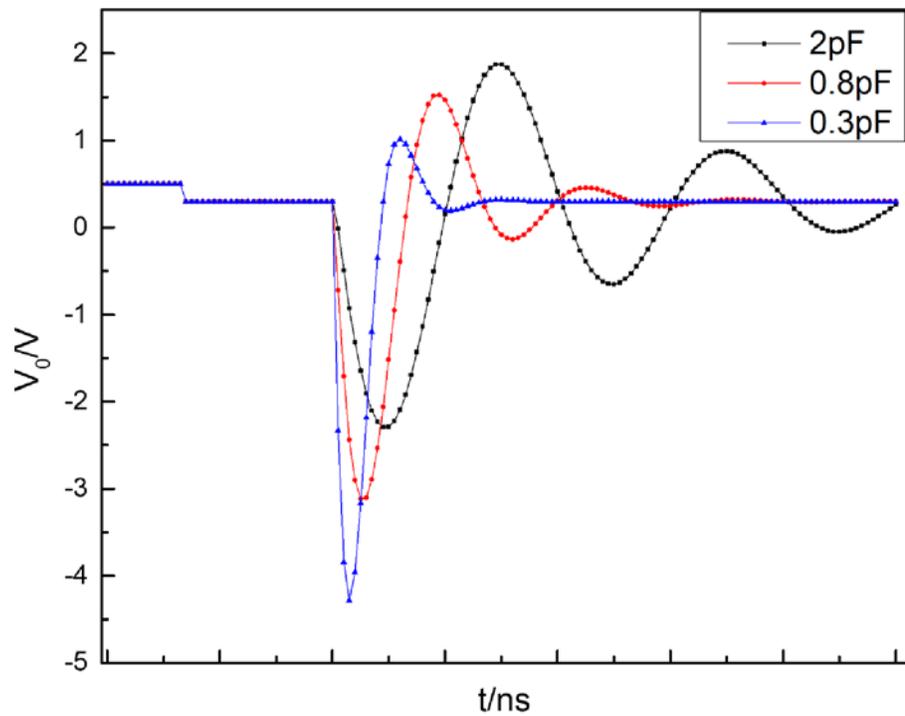
Fig 3(A) shows the amplitudes of  $V_0$  when  $L$  is 2nH, 5nH, and 10nH, respectively, for given values of  $C_d = 0.8$ pF,  $C_1 = 1$ μF, and  $R = 50$ Ω. Fig 3(B) presents the amplitudes of  $V_0$  when  $C_d$  is 0.3pF, 0.8pF, and 2pF, respectively, for given values of  $L = 2$ nH,  $C_1 = 1$ μF, and  $R = 50$ Ω. From Fig 3(A) and Fig 3(B), it can be concluded that the width, amplitude and shape of the generated pulse is largely dependent on the exciting inductance  $L$  and  $C_d$ . When other parameters are given, a small value of  $L$  means that the pulse width is narrow, the amplitude is small, and the pulse ringing is serious. When other parameters are given, a small value of  $C_d$  means that the pulse width is narrow, the amplitude is large, and the pulse ringing is slight. This conclusion indicates that the SRD with small junction capacitance ( $C_d$ ) is recommended for the circuit design, and the value of  $L$  should be chosen taking into account pulse width and amplitude.

### NLTL Circuit

Nonlinear transmission line (NLTL) is in a high impedance TEM uniform load on a transmission line consisting of varactor ladder network, which encompasses several micro-strip transmission lines with an interval of  $d$  [25]. Between the micro-strip transmission lines are the reverse bias Schottky diode, whose junction capacitance varies with the value of reverse bias. The structure of NLTL is shown in Fig 4(A). According to the micro-strip line principle, each section of the lossless micro-strip transmission line can be equivalently seen as a combination of distributed inductance and distributed capacitance. Fig 4(B) shows the equivalent circuit of NLTL, where  $L_0$  and  $C_0$  denote the distributed inductance and distributed capacitance of the lossless micro-strip transmission line, respectively,  $C_m(V)$  and  $R_m$  denote the junction capacitance and the parasitic series resistance of the Schottky diode, respectively.



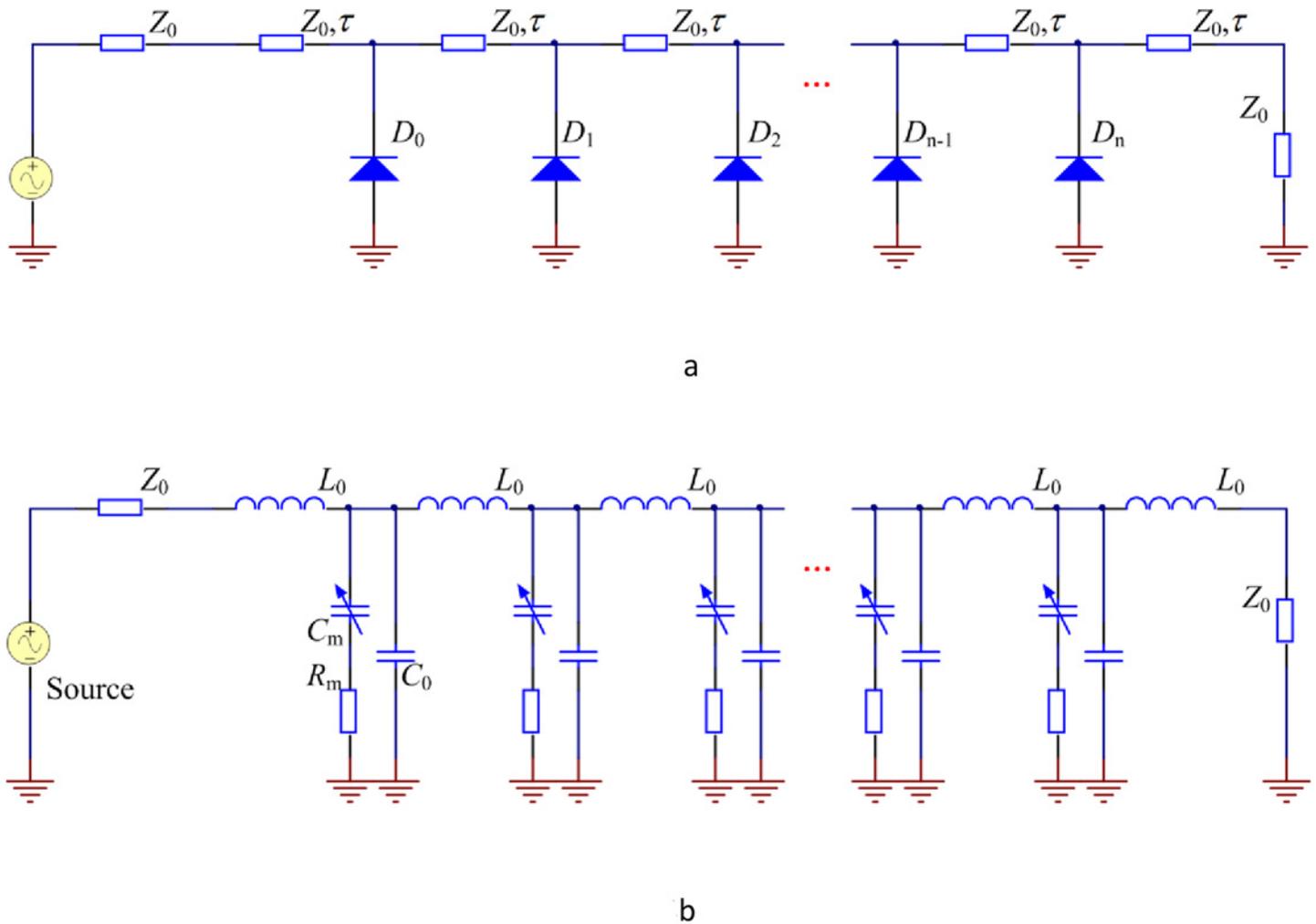
a



b

**Fig 3. Simulation curves of pulse production circuit.** (a)  $C_d = 0.8\text{pF}$ ,  $C_1 = 1\mu\text{F}$ ,  $R = 50\Omega$  (b)  $L = 0.2\text{nH}$ ,  $C_1 = 1\mu\text{F}$ ,  $R = 50\Omega$ .

doi:10.1371/journal.pone.0149645.g003



**Fig 4. Structure and equivalent circuit of NLTL.** (a) Principle diagram (b) Equivalent circuit.

doi:10.1371/journal.pone.0149645.g004

The network in Fig 4(B) can be seen as a low-pass filter, and the cutoff frequency is:

$$\omega_{\text{per}} = \frac{2}{L_0[C_0 + C_m(V)]} \quad (7)$$

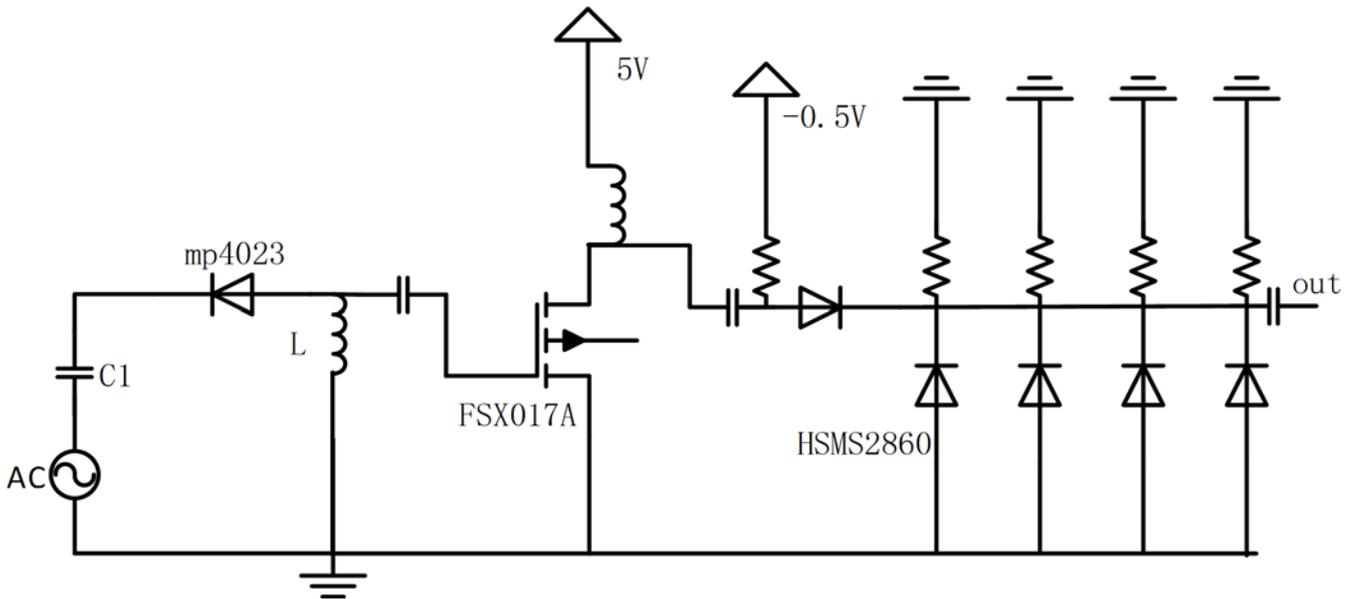
The operating frequency of NLTL is upper bounded by the cutoff frequency of the Schottky diode. Consider that  $R_m = 0$ , namely, the micro-strip line is lossless, and the voltage of the next node is:

$$V_o(t) = V_{in}[t - T(V)] \quad (8)$$

Where  $T(V) = \sqrt{L_0[C_0 + C_m(V)]}$

This equation demonstrates that NLTL's delay is related to the junction capacitance of the Schottky diode, which can be expressed as:

$$C_m(V) = \frac{C_{j0}}{\left(1 + \frac{V}{\phi}\right)^k} \quad (9)$$



**Fig 5. Principle diagram of pulse production circuit.**

doi:10.1371/journal.pone.0149645.g005

Where  $\phi \approx 0.4V$  (for HSMS-2820 Schottky diode),  $k$  denotes the coefficient of the diode and is usually in the range 1–3.

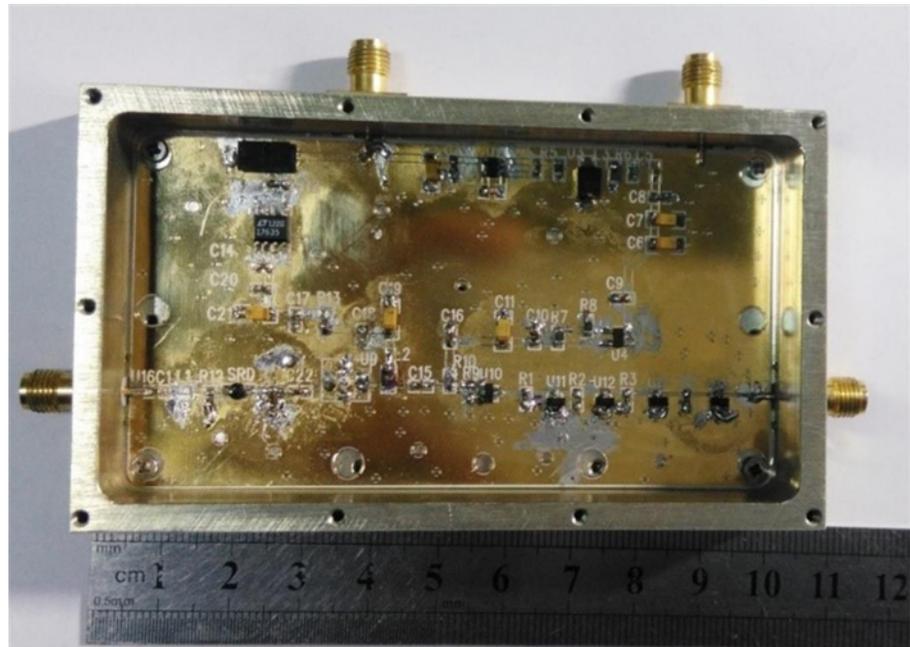
From Eq 1 and Eq 2, it can be known that the larger the value of reverse bias applied to the Schottky diode, the smaller the delay. For different voltages  $V_h$  and  $V_l$  ( $V_h > V_l$ ), the delay difference of NLTL for these two voltages is:

$$\Delta T = T(V_l) - T(V_h) = \sqrt{L_0[C_0 + C_m(V_l)]} - \sqrt{L_0[C_0 + C_m(V_h)]} \quad (10)$$

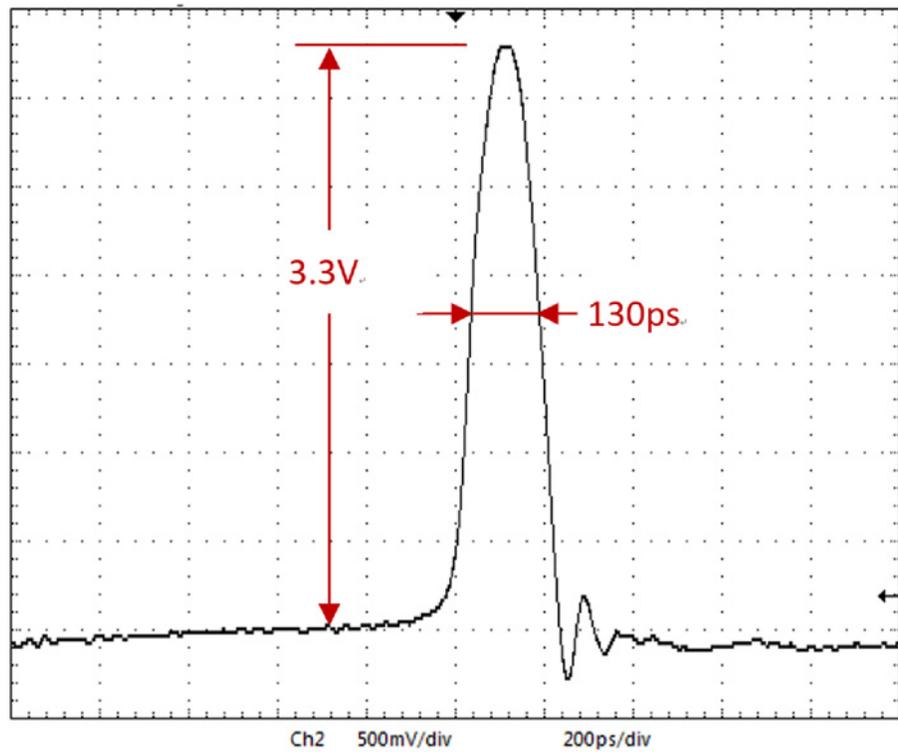
Therefore, when a forward narrow pulse passes through NLTL, the pulse rise time will be shortened, and the fall time will be lengthened. To shorten the falling edge time, a grounded resistance is added to each Schottky diode in NLTL, which can steepen the falling edge.

### Measurement Results and Discussion

According to the above analysis, the narrow pulse circuit consists of the SRD pulse-generating circuit and the NLTL circuit. As shown in Fig 5, at the left is the SRD pulse generating circuit, where SRD is of the type mp4023, with junction capacitance being  $C_d(-6V) = 0.5pF(max)$ , transit time  $t_t = 50ps$ , carrier lifetime  $t_r = 12ns$ ,  $C_1 = 1\mu F$ ,  $L = 5nH$ , and  $R = 50\Omega$ . On the right is the NLTL module used to further narrow the width of the pulse generated by SRD, where  $D_1 \dots D_4$  denote the Schottky diode,  $R_1 \dots R_4 = 50\Omega$ , the micro-strip transmission line length is 3mm, and the characteristic impedance of the transmission line is  $80\Omega$ . According to the actual test, the waveform of  $V_{out}$  is shown as in Fig 6. The circuit of the pulse generator is made utilizing Teflon boards. Fig 6(A) shows the prototype of designed pulse generator, the circuit structure of which is very compact. Furthermore, the waveform is monitored by Lecroy Wave Master 8600A 6GHz DSO oscilloscope as shown in Fig 6(B). The narrow pulse amplitude is 3.3 V and the pulse width is 130ps.



a



b

**Fig 6. Prototype and measured waveform of designed pulse generator.** (a) Prototype of designed pulse generator (b) Measured output pulse of the generator.

doi:10.1371/journal.pone.0149645.g006

## Conclusion

A narrow pulse-generating circuit is proposed based on SRD and NLTL. The influence factors in the pulse width and amplitude are discussed. Simulation results indicate that a small exciting inductance means that the amplitude of the generated pulse is small and the pulse width is narrow. The SRD with small junction capacitance will yield pulses with narrow width and high amplitude. Therefore, proper inductance and SRD with the smallest possible junction capacitance are recommended for UWB pulse-generated circuit design. To further reduce the width of the narrow pulse, the NLTL circuit is used, which can generate a narrow pulse with a half-amplitude width of 130ps and amplitude of 3.3V.

## Acknowledgments

This project is supported by the Chinese Defense Advance Research Program of Science and Technology, China (Grant No. 40404110203).

## Author Contributions

Conceived and designed the experiments: JZ QL. Performed the experiments: JZ FL. Analyzed the data: JZ FL YL. Contributed reagents/materials/analysis tools: YL QL FL. Wrote the paper: JZ QL.

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