Advanced Wafer Thinning Technology and Feasibility Test for 3D Integration

Y. S. Kim[a,b], N. Maeda[a], H. Kitada[a], K. Fujimoto[a], S. Kodama[a], A. Kawai[b], K. Arai[b], K. Suzuki[c], T. Nakamura[d], and T. Ohba[a]

[a] *School of Engineering, The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan*
[b] *DISCO CORPORATION, 13-11 Omori-Kita 2-chome, Ota-ku, Tokyo 143-8580, Japan*
[c] *Dai Nippon Printing Co., Ltd., 250-1, Wakashiba, Kashiwa-shi, Chiba 277-0871,Japan*
[d] *Fujitsu Laboratories Ltd.,10-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0197, Japan*

Introduction

The semiconductor industry is now facing a major turning point in how to realize the next generation of large-scale integration. Recently 3D integration (3DI) using through-silicon via (TSV) has widely studied and wafer thinning has been considered to be a promising technology for enhancing system performance instead of conventional two-dimensional (2D) scaling due to technical and economical issues. 3DI technology also provides benefits to reduce interconnect delay, form factor, and power consumption (Fig. 1). Moreover recent attention has focused on productivity and the costs involved in volume production. Wafer scale 3DI technology, so-called Wafer-on-a-Wafer (WOW), characterized by *thinning-first before bonding TSV-last* process and Cu multilevel TSV interconnects, has been developed [1, 2]. Stacking at the wafer level significantly increases the processing throughput, and low aspect ratio and “bumpless” TSVs give excellent contact yield as well as lower via stress (Fig. 2). There need further optimization of total thickness variation (TTV) in the stacking module. This paper describes high resolution grinding process for ultra-thinning using DGP8761 (DISCO) with *in-situ* thickness measurement (Auto-TTV, NCG = non-contact gauge). Wafer thinning effect for logic devices on mobility, gettering, and switching charge characteristics are discussed.

Results and Discussion

Figure 3 shows schematic diagram of grinding process. Wafer thickness uniformity after grinding is determined by contact angle between wheel and wafer surface. Since wafer is very slightly bowed and bonded on temporary adhesives, those uniformities reflect to the contact angle. In case of ununiform contact angle, thinned wafer thickness is varied resulting in large TTV (Fig. 3-a). With optimizing contact angle using Auto-TTV and NCG methods, lower TTV is achieved because wafer surface was adjusted geometrically to wheel head (Fig. 3-b). As a result, contact angle decides TTV reaching to 0.5 um of 300 mm wafer as shown in Figure 4.

With the ultra-thinning process, 300 mm wafer having 45-nm node high-performance logic device was evaluated, in which device has strained transistors and Cu/low-k multilevel interconnects. Silicon wafer was adhered onto support glass and thinned down to 7-um by conventional grinding and UPG. Since the hole mobility is more sensitive than that of electron for the channel strain [3], the external mechanical stress induces decreasing mobility in PMOS transistor. In this experimental, devices wafer was prepared by bonding, thinning and debonding process. It was found that the hole mobility of ultra thinned wafer down to 7-um was nearly same as that of before thinning for PMOS transistors. Thus the surface damage and the mechanical stress during wafer thinning process have no significant impact on the strained silicon transistors (Fig. 5). Figure 6 shows junction leakage current before and after thinning. Although the junction leakage currents slightly increase, those currents are negligible taking device specification into account. Wafer thinning, especially thinned down to near device layer, tends to involve metal contamination and reduce gettering sources, such as boron and oxygen precipitates (Fig. 7). If those defects reach to device region, device characteristics will be changed, e.g. junction leakage, threshold voltage, reliability, and retention time in memory. The gettering depends on types of wafer and thinning method. Usually epitaxially gown wafer is better than annealed wafer. Ultra-poly grind (UPG) is better than CMP method due to existence of non-crystalline layer which acts as extrinsic gettering site. In addition, gettering sensitivity of memory is higher than that of logic devices. In this experiment, we evaluated logic device on Epi-wafer and thinned using UPG. This is one of reason that only minimal change is shown in junction leakage. This also suggests that UPG process is adequate for the final treatment after grinding. In the case of FRAM device, negligible change of switching charge characteristic after wafer thinning down to 9-um was also observed (Fig. 8). According to those results, the electrical properties were not affected by ultra-thinning process, indicating applicable for thin-3D integration.

References

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* *corresponding author e-mail:* kimys@sogo.t.u-tokyo.ac.jp

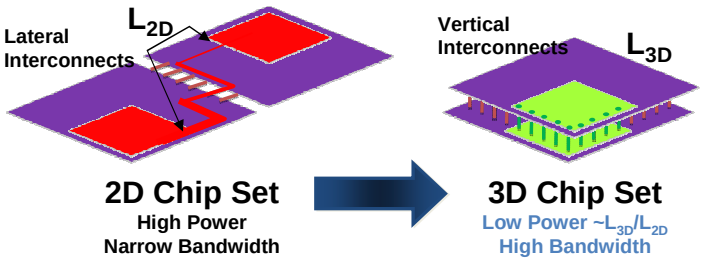


Fig. 1. Shift of scaling method from 2D to 3D Integration.

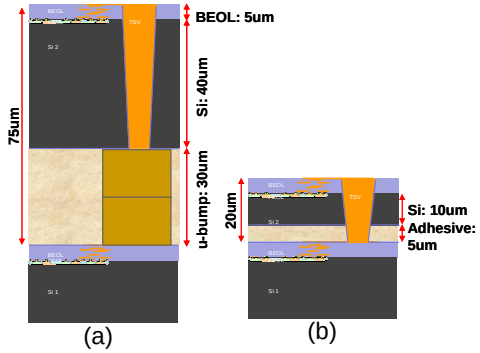


Fig. 2. Comparison of bonding method for (a) bump and (b) bumpless.

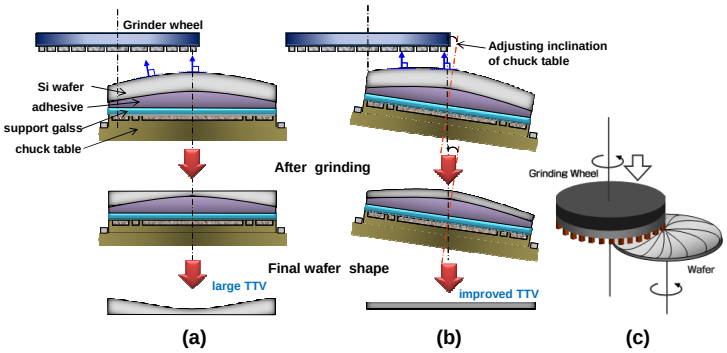


Fig. 3. Schematic diagram of Si wafer thinning: (a) ununiform contact angle, (b) optimizing contact angle by adjusting inclination of chuck table, and (c) infeed grinding which is conventional method for silicon wafer thinning.

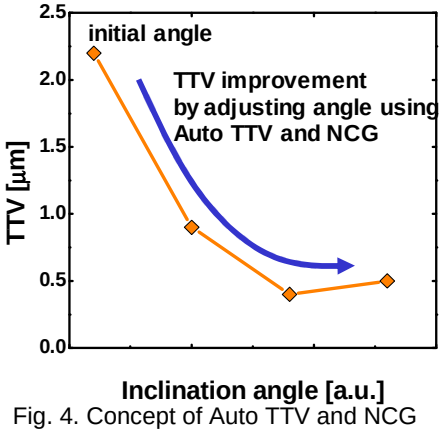


Fig. 4. Concept of Auto TTV and NCG for improving Si TTV by automatic sequence.

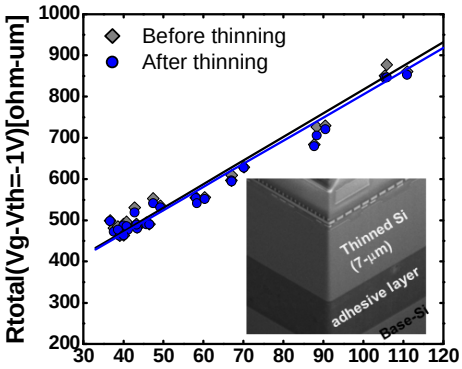


Fig. 5. Comparison of hole mobility for PMOSFETs before and after wafer thinning down to 7-um.

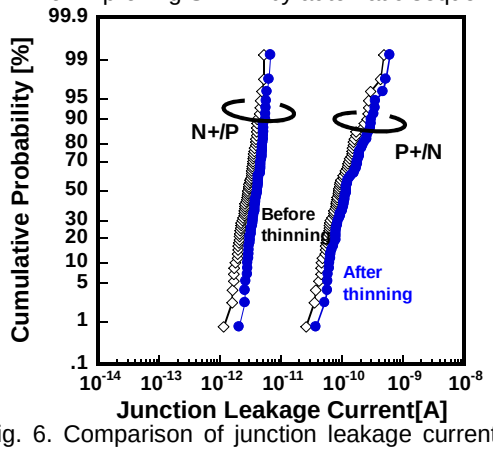
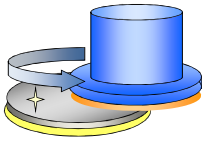


Fig. 6. Comparison of junction leakage current before and after wafer thinning.

Wafer thinning



- **metal contamination**
- **reduction of gettering source (boron and oxygen precipitates)**

Gettering effect

type of wafer	Epi-wf > Annealed-wf
thinning method	UPG > CMP

Gettering sensitivuty

type of device	Memory > Logic

Fig. 7. Process issues of wafer thinning, and gettering effects and sensitivity.

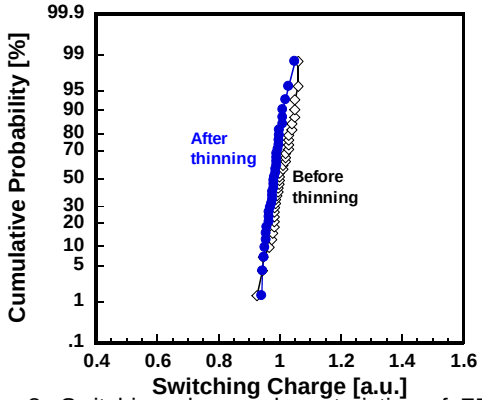


Fig. 8. Switching charge characteristics of FRAM before and after wafer thinning down to 9-um.