DC Hard Faults Detection and Localization in Analog Circuits Using Fuzzy Logic Techniques

Mohammed Merabet and Nacerdine Bourouba

Abstract— **This paper demonstrates a novel technique based on the use of a fuzzy logic system and the simulation before test (SBT) approach for hard faults detection and localization in analog electronic circuits comprising bipolar transistors. For this purpose, first, simulations of the circuit under test (CUT) are performed before the test stage by investigating the response of the circuit under test in faulty and fault-free conditions. Following this, two signatures parameters—output voltage and supply current—are observed and used for the fault diagnosis; the CUT is simulated using the OrCAD/PSpice software, and the output is analyzed in the DC domain. This method is validated through an inverter amplifier based on the uA741 operational amplifier. Then the results of different experiments are presented to demonstrate the applicability of the proposed method by increasing its efficiency.**

Index Terms— **Analog circuits, fuzzy logic, hard faults, fault detection, fault diagnosis, fuzzy inference system, simulation before test.**

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I. Introduction

THE subject of analog circuit fault diagnosis had gained popularity among researchers from the late 1970s to the early 1980s [1]–[2] due to the growing complexity of electronic circuits. Since then, fault detection and classification has been invoking a great deal of interest, becoming one of the largest domains of analog testing [3], [1]. However, it still faces some difficulties, e.g., in terms of inaccuracy of measurement, circuit nonlinearities, consideration of component tolerances, and poor fault models [4]. With respect to these difficulties, fuzzy logic seems to be one of the most effective tools that can be effectively employed to build an appropriate fuzzy inference system (FIS) that will have the potential to detect and locate faults depending on the inputs assigned to it.

A fault is a change in the value of a component with respect to its regular value that causes failure of the circuit. Faults in analog circuits are generally classified into two categories: hard faults and soft faults (i.e., catastrophic and parametric). Hard faults are attributed to short or open circuits; they lead to failures that manifest themselves in an altogether malfunctioning circuit [5]–[6]. Conversely, soft faults are those changes that hinder the performance of a circuit. This type of faults causes the parameters to deviate from their nominal value that can consequently leave their tolerance band [7]–[8].

Fault diagnosis in analog circuits is conducted using two broad approaches [4]: the simulation before test approach (SBT) and the simulation after test approach (SAT). SAT approach consists of calculating the circuit parameters from the measured responses obtained via the circuit under test (CUT) to observe if they exhibit the expected behavior [2], [9]. On the other hand, in the SBT approach, the response of the CUT is measured in the presence of a pre-selected set of faults, and the results are stored in a fault dictionary. The fault location is detected by comparing the circuit responses with the correspondents in the fault dictionary [9]–[10].

In this article, a strategy for hard fault detection and localization in analog circuits is presented, and a system based on fuzzy logic is used for this purpose. The proposed method is a part of the SBT approach, and experimental results indicate it has a high capacity. Moreover, using fuzzy logic makes it possible to distinguish between different faults even if their values are very close to each other; therefore, the ambiguity rate is zero.

II. Fault Detection and Localization Algorithm

To locate faults, the following successive steps have been assumed:

1) Simulation of the CUT in the DC domain.
2) Extraction of the output voltage and supply current for fault-free and other faulty conditions.
3) Creation of the fault dictionary.
4) The parameters extracted from the fault dictionary are presented as inputs in a fuzzy logic system that detects and localizes the fault.

The block diagram for the proposed approach has been illustrated in Figure 1.

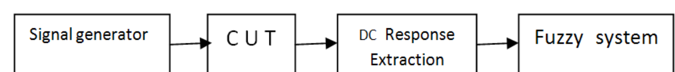

Fig. 1. Block diagram of the proposed algorithm.

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III. Fuzzy Logic Approach

The fuzzy approach is used to localize hard faults in analog circuits; these faults are caused by open or short components in bipolar transistors [11]. A fault dictionary is a priori produced by collecting signatures of different fault conditions that are simulated in the DC domain. A FIS is utilized to process the CUT's response.

The basic architecture of a fuzzy logic system is shown in Figure 2.

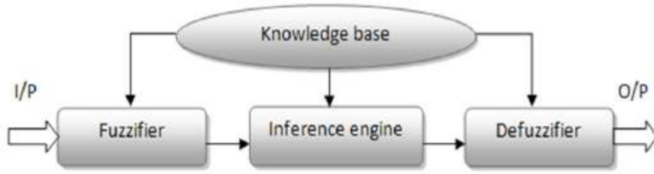


Fig. 2. Basic architecture of a fuzzy system.

The main component of fuzzy logic is the fuzzifier, which transforms real value inputs into members of fuzzy values by applying the membership functions of the fuzzy knowledge base [12]. Several types of membership functions can be used for the fuzzification process, such as triangular, trapezoidal, and Gaussian membership functions. The triangular shape has been used in this work. This function is frequently encountered in practice—e.g., [9]–[10], [13], [16]—given its efficiency with respect to calculation time. This efficiency can be attributed to its simple structure consisting of simple straight-line segments.

The inference engine takes the fuzzy input and converts it into fuzzy output by applying IF-Then type fuzzy rules (Figure 3). The process of converting the fuzzy output of the inference engine into a crisp value is called defuzzification [3].

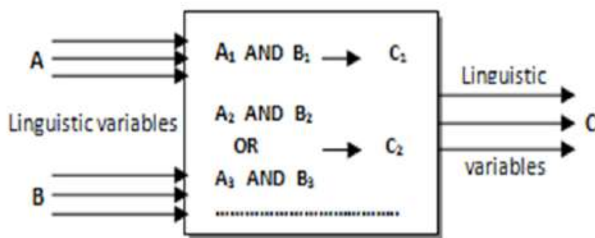


Fig. 3. Fuzzy inference process.

There are a number of defuzzification methods [3], [9], such as centroid of area (COA), bisector of area (BOA), mean of maximum (MOM), smallest of maximum (SOM), and largest of maximum (LOM). Centroid defuzzification (COA) is the most commonly used method, as it is very accurate [10], [12]. The defuzzified values obtained through COA, unlike the values obtained through other methods, divide the area under the membership function into two equal parts (see Figure 4), which can directly compute the crispest value of the fuzzy quantity [10].

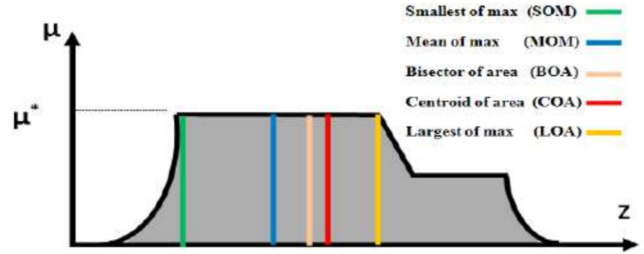


Fig. 4. Defuzzifying methods.

Although there are mainly two types of fuzzy inference methods, namely, Mamdani and Sugeno methods, the Mamdani method was chosen to create the FIS due to the transparency of its rules between the inputs and outputs and its simple implementation steps [13]. It allows us to describe the knowledge in a more intuitive and human-like manner [9]. As opposed to the Sugeno model, the Mamdani model expresses the output using fuzzy terms instead of mathematical combinations of the input variables.

Mamdani uses an inference strategy that is generally termed as the max-min method. The format of the rule base for the Mamdani fuzzy systems has been provided below:

Where x_{pi} (p = 1, 2, 3 … n) is the input, y_l is the output of fuzzy rule, and A_{pl} (p = 1, 2, 3 … n) is the fuzzy membership function that is associated with linguistic variables. Figure 5 illustrates the max-min composition and centroid defuzzification methods [9], which have been used in this study.

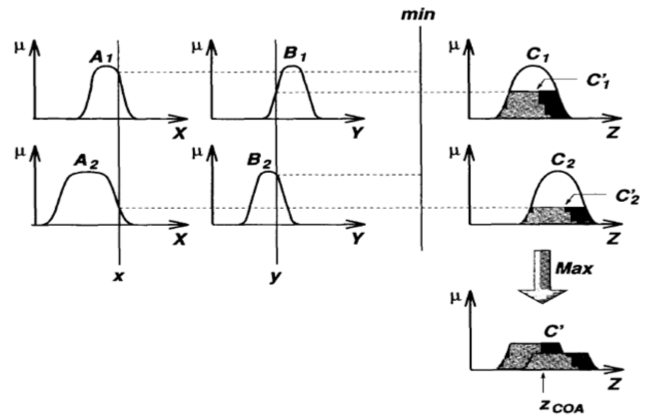


Fig. 5. Max-min composition and centroid defuzzification.

IV. Experiments And Results

To verify the feasibility of the proposed approach, we apply the steps mentioned in Section II to the operational amplifier uA741, which is operated in an inverting configuration and widely employed as building block components for many analog systems [14]. The simulation circuit is then simulated using the PSpice software. The data obtained from these simulations was transferred to the MATLAB environment for use in the building of the FIS system. Additionally, the fuzzy toolbox was used to locate faults, as described below.

A. Inverting Amplifier Circuit

Figure 6 depicts the configuration of an inverting amplifier. The closed-loop gain of the amplifier is set by two resistors: the feedback resistor, R2, and the input resistor, R1. The component parameters are R1 = 1 k and R2 = 4.7 k. Figure 7 demonstrates the transistor-level circuit of the uA741 amplifier that was used in this study. The chosen test vector includes the input voltage signal whose value ranges from − 5V to + 5V, which represent the limit values that can be accepted by the circuit and whose variation step is sufficient and necessary to explore the fault's effect.

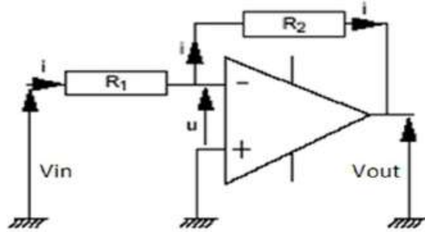


Fig. 6. Inverting amplifier.

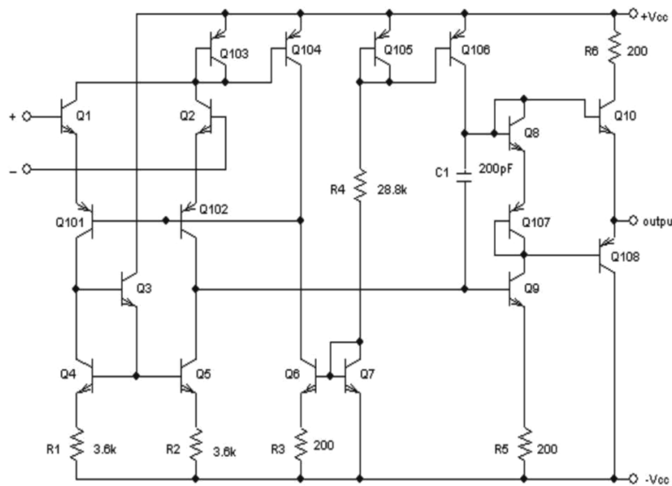


Fig. 7. The uA 741 operational amplifier circuit at the transistor level.

B. Faults Applied

In this experiment, the faults that were considered were mostly short circuits and open circuits, which were applied to the active components (transistors). The short circuits were materialized by resistors of low values (1 Ohm), whereas open connection lines or resistors with high value (100 Mohm) were used for the open circuit [15]. Therefore, for each transistor in the circuit, six faults have been included in the fault list as illustrated in Figure 8 and as listed as follows:

- emitter contact open (EO);
- collector contact open (CO);
- base contact open (BO);
- base to collector short (BCS);
- base to emitter short (BES);
- collector to emitter short (CES).

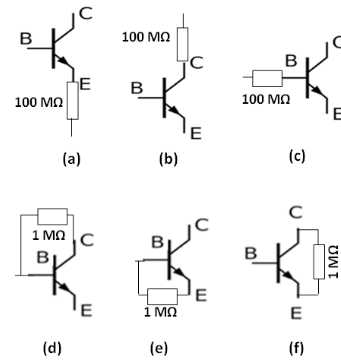


Fig. 8. Open and short transistor faults.

The inverting amplifier is an assembly of 18 transistors and, as the number of faults specific to each transistor is 6, these many components leads to the observation of the effects of 108 theoretical faults. However, the number of faults was reduced to 70 due to its electronic configuration:

- Some short or open faults measured individually at the level of an element are considered to be a duplicate fault because they affect another element that shares a common node with the first.
- Other short circuits associated with the same transistor are considered to be duplicate faults due to the way this element is connected in the circuit; for example, the diode element Q7 (shorted B-C junction) affects a short between B and E and is also treated as a short between E and C.

C. Building the Fault Dictionary

1. Output Voltage: A priori, the analysis of the transfer function is performed to detect the test vector (stimulus) at the input that allows the effect of faults to propagate to the output. The following findings will clarify this procedure:

- The input voltage range and measurement of the corresponding output voltage can be applied to reproduce the transfer characteristic (see Figure 9).
- This task is taken up by a set of faults that are yet to be explored to measure the characteristics of the circuit under its different fault conditions, some of which are presented in Figure 10.

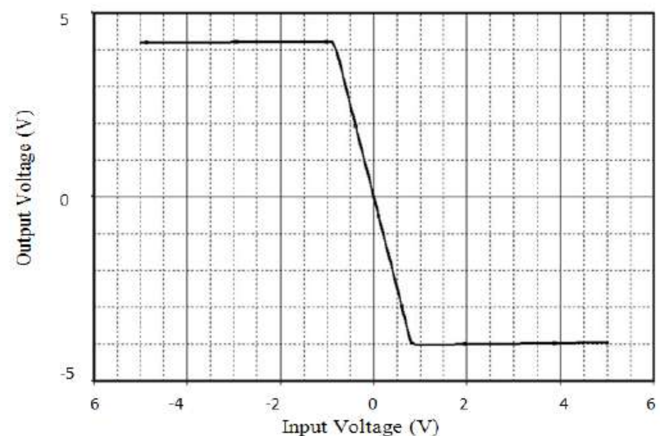
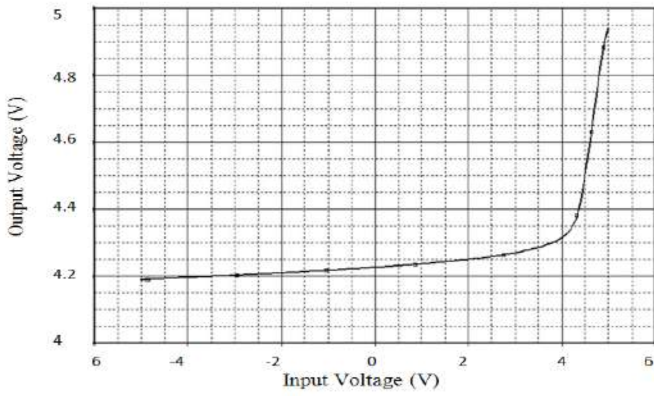
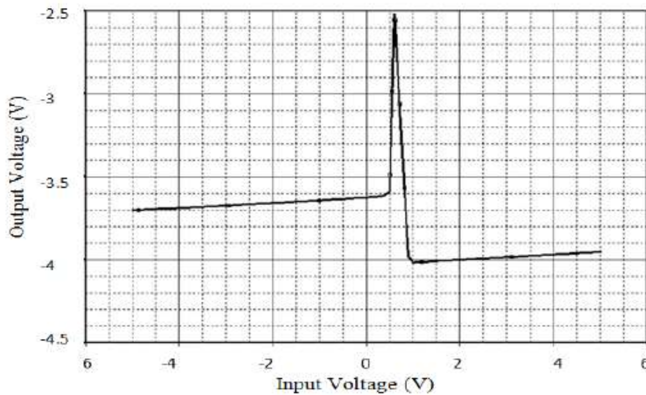


Fig. 9. Transfer function of the circuit for fault free.



(a)



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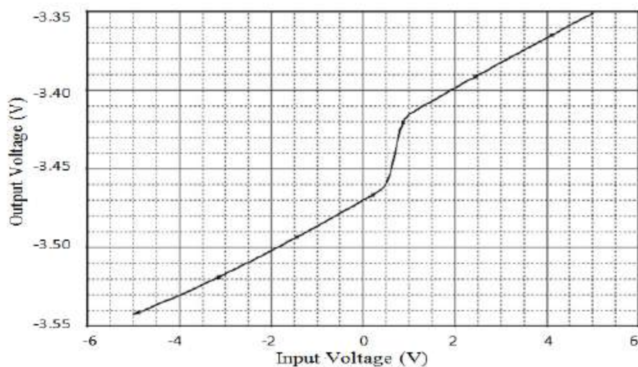


(c)

Fig. 10. Transfer function of the circuit for some fault conditions: (a) BOQ101 (b) BESQ8 (c) BCSQ10.

2. Supply Current: The power supply current test applied to the inverting amplifier consists of measuring the current at the negative power supply to ensure that faults that were not detected by the first mode test (output voltage) are detected. The same test vectors that were used in the previous test were imposed here.

Figures 11 and 12 demonstrate the simulation results of the good circuit and the faulty circuits, respectively. The supply current has been plotted with respect to the input voltage *Vin.*

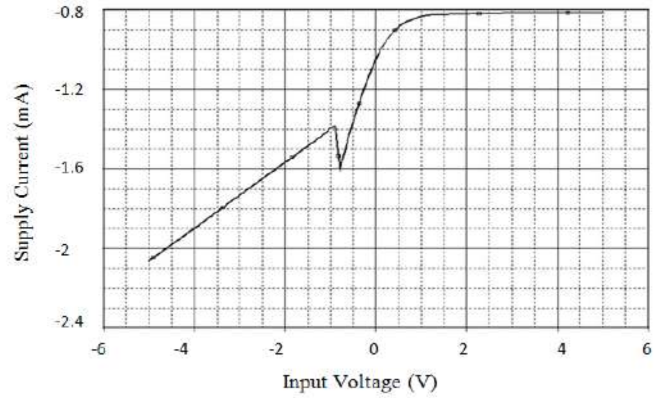
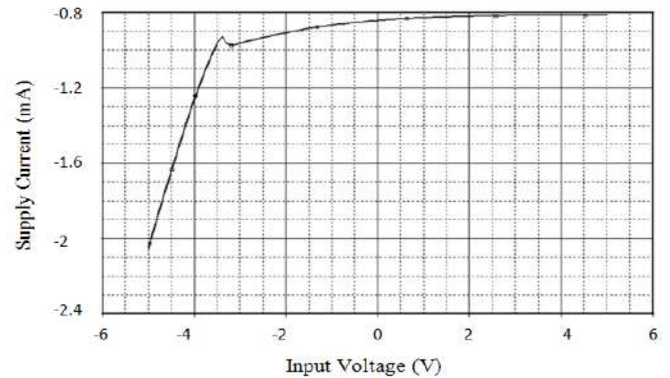
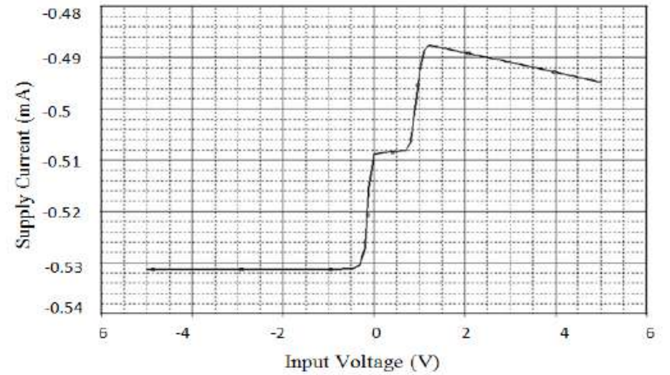


Fig. 11. The supply current plots in terms of the input voltage.



(a)



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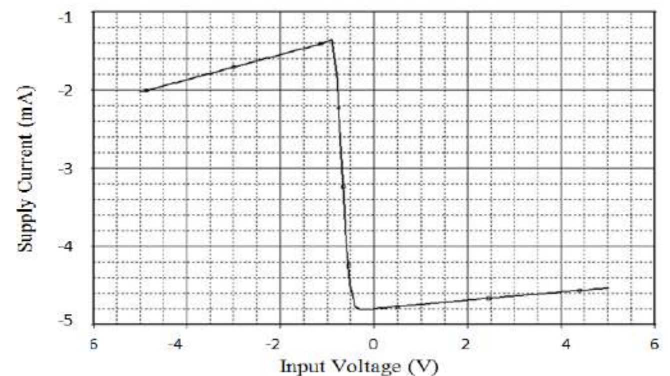

(c)

Fig. 12. Supply current of the circuit for some fault conditions: (a) CESQ3 (b) EOQ2 (c) ECSQ107.

The faults dictionary that was constructed has been depicted in Table I. The results concern the fault coverage evaluation obtained using the classic method. The criterion on which this method is based is defined as a deviation of +/- 1.5% from the nominal value for the two fault analysis parameters (the supply current and the output voltage). This implies that any fault is considered to be detected if it produces a deviation on the nominal value of one of these parameters, which is equal to or greater than this tolerance value. Such a tolerance choice is made from the concept of a current or voltage meter for laboratory use, requiring a precision class of no more than 1.5%. This resulted in a 78% fault coverage by using output voltage as a fault signature. An improvement in this fault detection rate was achieved by implying the supply current as the second fault signature—the combination of these two parameters allowed the detection of 85% faults.

Table 1. Fault Dictionary Of The Inverting Amplifier Circuit

Fault ID	Fault conditions	Output Voltage(V)	Supply Current(mA)	FIS Output
f0	FF	-3,9424	-0,8489	0
f1	**BOQ1**	**-4,0182**	-0,8306	1.1
f2	**COQ1**	**-4,0111**	-0,8531	2.06
f3	**BOQ2**	**4,236**	-1,1036	2.95
f4	**COQ2**	**-3,5003**	-0,8756	3.98
f5	**BOQ3**	**-3,9924**	-0,8407	5.02
f6	**COQ3**	**-3,9919**	-0,8568	6.05
f7	**BOQ4**	**-2,9597**	-0,8573	7.15
f8	**COQ4**	**-3,5118**	-1,0312	8.05
f9	**BOQ5**	**-3,9707**	-0,7608	8.99
f10	**COQ5**	**-3,9732**	-0,8307	10.1
f11	**BOQ6**	**4,236**	-0,8705	11
f12	**COQ6**	**4,236**	-0,8708	12.1
f13	**BOQ7**	**-3,7581**	-10,008	13
f14	**COQN7**	**-3,9957**	-0,9774	14.05
f15	**BOQ8**	**-3,5436**	-6,473	15.1
f16	**COQ8**	**-4,0209**	-0,83	16.1
f17	**BOQ9**	**4,2359**	-0,9567	17
f18	**COQ9**	**4,2358**	-1,066	18.2
f19	**BOQ10**	**-3,938**	-0,8202	19
f20	**COQ10**	**-3,9652**	-0,8207	20
f21	**BOQ103**	**4,2352**	-0,9752	20.99
f22	**COQ103**	**-3,6747**	-0,8012	22.02
f23	**BOQ104**	**-3,868**	-3,8562	23.1
f24	**COQ104**	**-3,868**	-3,8563	24.05
f25	**BOQ105**	**3,9108**	-4,7673	25
f26	**COQ105**	**-3,8371**	-1,1471	26
f27	**BOQ106**	**-4,1335**	-0,5057	26.98
f28	**COQ106**	**-4,1336**	-0,5066	28.1
f29	**COQ107**	**-3,9429**	-0,8897	29
f30	**BOQ108**	**0,7821**	-0,8047	30.02
f31	**COQ108**	**-3,5723**	-0,8226	31
f32	**BCSQ1**	**1,1978**	-116,873	32.1
f33	**BESQ1**	**-3,6525**	-4,0572	33.1
f34	**CESQ1**	**4,236**	-1,1124	34.05
f35	**BCSQ2**	**4,3241**	-3,7096	35
f36	**BESQ2**	**-3,9472**	-0,8389	35.9
f37	**CESQ2**	**-4,0163**	-0,8426	37
f38	**BCSQ3**	**4,2143**	-1,1517	38
f39	**BESQ3**	**-3,9924**	-1,1447	39.1
f40	**BCSQ4**	**-3,9585**	-0,8308	40
f41	**BESQ4**	**-3,9923**	-1,7371	41.1
f42	**CESQ4**	**-3,9914**	-0,8305	42
f43	**BCSQ5**	**0,2217**	-56,044	42.9
f44	**CESQ5**	**1,3334**	-66,861	44
f45	**BCSQ6**	**-2,9332**	-53,567	45.1
f46	**BESQ6**	**4,2359**	-0,8925	45.9
f47	**CESQ6**	**-3,1548**	-25,823	47
f48	**BESQ7**	**4,2359**	-0,8947	48
f49	**BESQ8**	**-3,9367**	-0,8228	49.1
f50	**BCSQ9**	**-3,4253**	-0,8481	50
f51	**CESQ9**	**-4,1369**	-0,8491	51
f52	**BCSQ10**	**3,4321**	-4,7524	52.05
f53	**BESQ10**	**-4,096**	-0,825	53
f54	**CESQ10**	**2,1206**	-15,167	54
f55	**BCSQ101**	**-3,3445**	-11,241	55
f56	**BESQ101**	**-0,0297**	-0,8869	56.2
f57	**CESQ101**	**-3,0194**	-16,107	57
f58	**BCSQ102**	**-2,2499**	-16,667	58
f59	**BESQ102**	**4,2359**	-0,9569	59.3
f60	**CESQ102**	**-2,0382**	-15,561	60
f61	**BESQ103**	**-3,8677**	-3,8572	61.05
f62	**BCSQ104**	**4,236**	-0,9716	62.1
f63	**CESQ104**	**4,236**	-0,9719	63
f64	**BESQ105**	**-4,1347**	-0,5416	64.2
f65	**BCSQ106**	**3,4074**	-4,7131	64.9
f66	**CESQ106**	**4,2232**	-4,8967	66
f67	**BESQ107**	**-3,9367**	-0,823	67.1
f68	**BCSQ108**	**-4,2057**	-0,8491	67.9
f69	**BESQ108**	**4,1556**	-3,0547	69
f70	**CESQ108**	**-5**	-6,6342	69.98
number of faults (detected/ injected)		55/70	60/70	70/70

However, there were problems that arose that need to be resolved. These problems include 15% of faults escaping this test mode (f9, f10, f14, f20, f29, f39, f41, f42, f49, f67) and the indistinguishable detected faults constituting groups of ambiguous faults such as (f11, f12, f62, f63), (f5, f39), (f23, f24), making it more difficult to locate them. The data of this dictionary is processed via the FIS to provide solutions to these problems. These solutions have been detailed in the following sections.

D. Simulation Results

All hard faults have been obtained from the DC response and tabulated in Table I. The faults have been coded and can be identified through the following abbreviations: EOQn, BOQn, COQn, EBSQn, ECSQn, and BCSQn, where E, B, and C, respectively, denote the emitter, the base, and the collector of the transistor, which can be identified by the letter Q and its position number n in the configuration. From the simulation results (Table I), it can be seen that the output voltage and supply current are different for different fault conditions. The extracted features are then fed as inputs into the FIS.

The FIS that has been suggested to solve the problem of fault detection and localization is shown in Figure 13. It has been created through three steps [3], which have been listed as follows: defining the input membership function (output voltage and supply current), defining the output membership functions and, finally, creating the rule base.

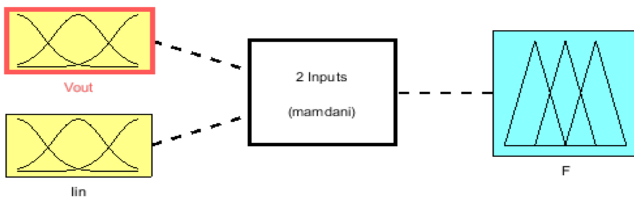

Fig. 13. Mamdani fuzzy inference system (two inputs).

The values of the input parameters are divided into different intervals according to different fault groups. After a number of experiments, this distribution has led to a suitable choice of 18 intervals for the output voltage parameter (Figure 14) and 7 for the supply current parameter (Figure 15). Each value region undergoes a transformation into linguistic parameters, which are provided as input in Madani's FIS. We would like to remind that for each of these regions, a triangular membership function TMF is assigned.

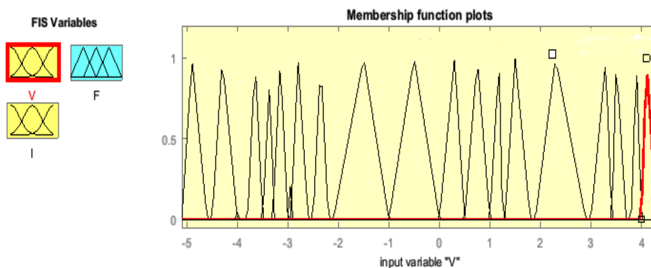

Fig. 14. Membership function of output voltage.

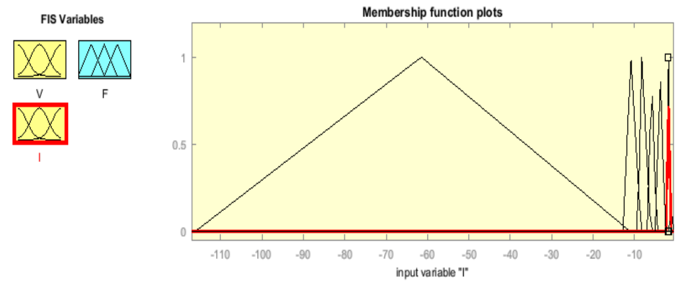

Fig. 15. Membership function of supply current.

The output membership functions are also assigned to the output variables; the membership function is divided into areas, as shown in Figure 16, that characterize the different faults' identities, which can be obtained using the fuzzy rule base. As there are 70 different configurations of the CUT in the fault dictionary, there must be 70 fuzzy rules for the problem under consideration. The fuzzy rule base defines the relationship between the input and the output fuzzy sets. As a result, the use of fuzzy IF-THEN rules imitates the ability of the human mind to make decisions [13]. Finally, the centroid defuzzification method was used on the fuzzy set "fault" to obtain a crisp value, which can be used to easily identify the faults. The output of the FIS for the given inputs is demonstrated in Figure 17.

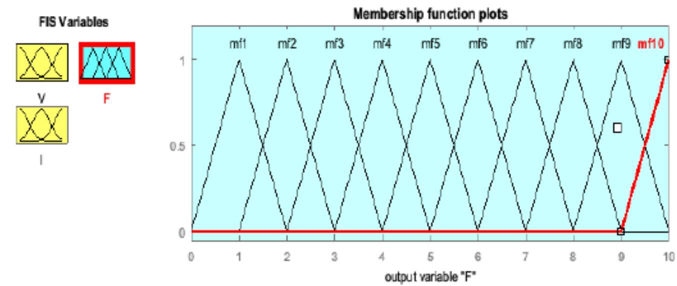

Fig. 16. Membership Function for Fault ID (display range [0 10]).

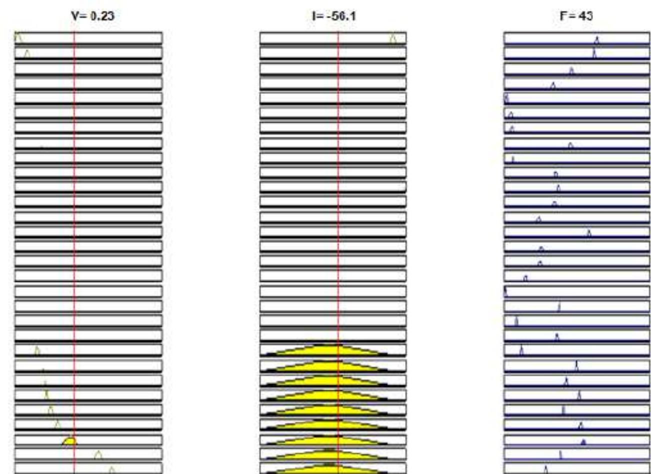

Fig. 17. Output of the FIS.

The fault case F18 has been chosen to illustrate the approach. The FIS for index fault 18 (F18) is 4.2358, − 1.066. For

this input, the triangular membership functions (TMF) for the output voltage and supply current are 4.1, 4.23, 4.5 and − 1.2, − 1, − 0.8, respectively.

The TMF for the output is defined as 17, 18, 19 by setting the fault index (in this case, 18) as the center of the TMF. The fuzzy rule for this fault has been provided as follows:

"If V_{out} is in the range 4.1 to 4.5 and I_{in} is in the range − 1.2 to − 0.8, then the fault range is 17 to 19."

The FIS output has a value of 18.2 after defuzzification whose rounded number corresponds to the defect index 18 as a fault identifier (fault ID).

To support the practicality of the approach, the results of some fault cases have been resumed in Table II and agree well within the corresponding fault ID.

Table 2. FIS Inputs and Outputs for Test Cases F4, F49, and F52.

Fault ID	Input FIS		TMF output voltage		TMF supply current		TMF output	FIS output
F4	[-3,5003 -0,8756]	IF	[-3.6 -3.5 -3.4]	AND	[-1 -0.7 0]	THEN	[3 5]	3.98
F49	[-3,9367 -0,8228]		[-4 -3.8 -3.6]		[-0.9 -0.75 -0.7]		[48 50]	49.1
F52	[3,4321 -4,7524]		[3.3 3.4 3.5]		[-5 -4.5 -4]		[51 53]	52.05

The same applies to other faults where the input and output TMF are determined from the values of the output voltages and supply current and the fault index, respectively.

The FIS outputs exhibited in Table I clearly indicate that the totality (100%) of faults being investigated in the present work have been detected and successfully dispatched to each other. This has been conducted on zero groups of ambiguous faults and, thus, will help in a good fault location.

To verify the efficiency of the method proposed in this paper, Table III compares the fault coverage of the proposed method with that of the classical test method and an earlier method [16] using the time-mode simulation for the same circuit. The fault coverage is found to be 100% for the proposed technique, whereas for the classical testing and time-mode testing method, it is not more than 90%.

Table 3. Comparison of Fault Coverage for Proposed Method, an Earlier Method [16] and Classical Test Methods.

Earlier method [16]	Classical test		Proposed method
	Output voltage	Supply current	
Fault coverage			
90%	78%	85%	100%

V. Conclusion

This paper applies fuzzy logic in the detection and localization of hard faults in analog circuits in the DC domain.

The FIS can display the diagnostic result visually and directly. Moreover, the results presented in this research work are very conclusive, as 100% of the entire volume of faults being examined was detected using both DC supply current and output voltage as the fault signature parameters.

Furthermore, applying the FIS approach as the fault classification tool has led to more accurate fault location in comparison to the aforementioned approaches, as all the examined faults had been successfully dissociated from each other.

This experiment indicates that this technique can quickly detect hard faults in analog circuits, as it requires one DC input voltage (a single test vector) instead of an entire voltage range. Our future work will focus on expanding the proposed approach to other analog circuits.

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