R.E. Bryant proposed a method to handle logic expressions [3], which is based on binary decision diagrams (BDD) with restriction: variable ordering is fixed throughout a diagram. Although the method has much more efficiency than other methods proposed so far, the efficiency heavily depends on variable ordering. We developed a simple but powerful algorithm for variable ordering. The algorithm tries to find a variable ordering which is very natural, i.e., minimizes the number of crosspoint of nets, when the circuit diagram is drawn. We applied this to the boolean comparison of ISCAS benchmark circuits for test pattern generation. The results show that BDD with our ordering method can verify almost all benchmark circuits in less than several CPU minutes, which is one hundred times or more faster than those reported in the literature. We also mention some techniques for circuit evaluation orderings.

References
Logic Verification using Binary Decision Diagrams in a Logic Synthesis Environment

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Abstract

This paper presents the results of a formal logic verification system implemented as part of MIS, the multi-level logic synthesis system developed at U. C. Berkeley. Combinational logic verification involves checking two networks for functional equivalence. Techniques that flatten networks or use cube enumeration and simulation cannot be used with functions that have very large cube covers. Binary Decision Diagrams (BDDs) as presented by Bryant are canonical representations for Boolean functions and offer a technique for formal logic verification. However, the size of BDDs is sensitive to the variable ordering. We consider ordering strategies based on the network topology. Using BDDs, we have been able to carry out formal verification for a larger set of networks than existing verification systems. Also, this method proved significantly faster on the benchmark set of examples tested.

References

BEAT_NP: A Tool for Partitioning Boolean Networks

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Abstract

BEAT_NP (BooLEAn Tools Network Partitioner) was designed to extend the application size capability of the BOLD (Boulder Optimal Logic Design) system. BEAT_NP partitions a Boolean Network into subnetworks which satisfy user specified size constraints. Because most of the tools in the BOLD tool suite solve problems which are in NP or Co-NP, they may be assumed to have exponential complexity. Because the BEAT_NP algorithms have log-linear worst case complexity, the cpu time requirements of optimization tools can be reduced greatly in difficult cases. When used with the BOLD minimizer on a set of well known benchmark examples, BEAT_NP has been found to reduce cpu time by 1 to 3 orders of magnitude while retaining a significant majority of the optimization savings available in the unpartitioned case.

References

An Efficient Macromodeling Approach for Statistical IC Process Design

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Abstract

This paper describes an efficient macromodeling approach for statistical IC process design based on experimental design and regression analysis. Automatic selection of the input variables is done as part of the model building procedure to reduce the problem dimension to a manageable size. The resulting macromodels are simple analytical expressions describing the device characteristics in terms of the fundamental process variables. The validity and efficiency of the macromodels obtained by the approach are illustrated through their use in an IC process device design centering example.

References

iEDISON: An Interactive Statistical Design Tool for MOS VLSI Circuits

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ABSTRACT

This paper presents a design tool iEDISON for the statistical optimization of MOS VLSI circuits. It optimizes the transistor sizes of a circuit so that its performance is least sensitive to the manufacturing process fluctuations. iEDISON considers three methods for design optimization, namely, the response surface method, the Taguchi method, and the non-nested experimental design method. These methods use experimental designs and regression models to explore the statistical performance variations. The efficiency of the system is demonstrated by an example on clock skew minimization.

REFERENCES

An Efficient Method for Circuit Sensitivity Calculation Using Piecewise Linear Waveform Models

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ABSTRACT

This paper presents an efficient method for calculating the transient sensitivities in MOS circuits with respect to a large number of parameters. The approach employs simple circuit models built with piecewise-linearization of time-domain circuit responses. Closed-form expressions are derived for the calculation of transient sensitivities of the corresponding linear circuits. The transient sensitivity of the nonlinear circuit is then approximated as a simple function of individual linear circuit sensitivities. It is shown that the efficiency of this approach increases with the circuit size as well as with the number of sensitivity parameters considered.

REFERENCES
**Codar: A Congestion-Directed General Area Router**

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**Abstract**

A general area router that integrates the phases of global routing and detailed routing has been developed. The global phase coarsely places the nets based on the congestion of the routing region, and the detailed phase modifies the coarse wiring to find legal positions for all wire segments. Both phases employ the same grid-space of routing tracks with two or more levels of interconnect. With this integrated data structure, the router can alternate between global and detailed routing operations, both of which employ rip-up and reroute techniques. This integration has resulted in a router that can solve difficult problems not solvable by other programs while exhibiting run-times that grow only moderately with the size of the routing problem.

**References**

CARIOCA - A "Smart" and Flexible Switch-Box Router

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Abstract

A two dimensional router utilizing two layers is presented. The routing technique we have implemented can roughly be described as follows:

After partitioning of the nets into a set of subnets, the construction is carried out on a step by step basis, which allows the system to dynamically take into account new information on the problem. This part has been implemented with a blackboard architecture.

The router can handle pins that are not on a grid on one set of parallel edges.

In order to always provide a solution to a given problem, the router expands the switch-box by adding rows dynamically where they are needed. This point will be justified.

Many test cases have been run successfully and some results, including Burstein's difficult switch-box, are presented.

References

A Detailed Router Based on Simulated Evolution

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ABSTRACT

This paper presents a representation scheme for a rip-up and rerouter. The status of the routing region is represented as a four dimensional matrix. Rip-up and re-route operations are emulated as matrix subtractions and additions, respectively. The quality of a routing result can be measured by performing a few simple matrix operations. A rip-up and reroute switch-box/channel router, called SILK, using simulated evolution technique has been implemented based on this representation scheme. Experimental results showed that SILK, when solving all the classical benchmarks available to us, out performed WEAVER, the most successful switch-box router to date, in both quality and speed aspects.

REFERENCES

Automatic Synthesis of a Multi-Bus Architecture for DSP

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ABSTRACT

A novel architectural synthesis methodology for a multibus multi-functional unit processor is presented. It is implemented as part of a design aid tool called SPAID. The input to SPAID is a DSP flow graph algorithm description with the required throughput and latency. The synthesized processor is a self-timed element externally, while it is internally synchronous, suitable for a systolic multi-processor implementation for large DSP applications. For a benchmark elliptic filter algorithm SPAID synthesizes architectures with a linear topology that use less interconnects and multiplexers than other systems synthesizing random topology architectures for the same throughput.

REFERENCES

Area-Time Model for Synthesis of Non-Pipelined Designs

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Abstract

The ability to predict area-time characteristics of designs without actually synthesizing them is vital to producing quality designs in a reasonable time. In this paper, we give a mathematical model for predicting the area-time tradeoff curve for non-pipelined datapaths given a data flow graph and a module set. The model has been validated against designs generated by a program which synthesizes non-pipelined datapaths.

References
Constrained Conditional Resource Sharing in Pipeline Synthesis

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ABSTRACT

This paper presents a conditional resource sharing algorithm for pipeline synthesis that allows sharing of hardware components among the mutually exclusive parts of any conditional branches appearing in a behavioral description. If done improperly, resource sharing in a conditional may increase excessively the critical path delay of the conditional, hence causing performance degradation. Given area/time constraints for a pipelined design, finding an optimal conditional sharing solution is a combinatorial optimization problem. Our algorithm uses heuristics with a user-defined weight that trades off area versus time such that the algorithm is either manually or automatically iterated by changing the weight until a solution close to the target is obtained or it is determined that it is impossible to obtain. The algorithm is interactive so designers can manually determine partial or whole sharing.

REFERENCES
Combining Event and Data-Flow Graphs in Behavioral Synthesis

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Abstract

The behavioral specification of a digital circuit consists of two parts: its internal behavior (data-flow and operations) and its interface behavior (signaling conventions and their timing constraints). Current behavioral synthesis systems use data-flow graphs to represent internal behavior. Recently, specialized synthesis systems have been developed that use event graphs to address the special nature of interface behavior. Combining event and data-flow graphs into a single unified representation has implications for how digital circuits are described and synthesized. This paper presents a new unified behavior graph and outlines the new algorithms required to support automatic synthesis. The new descriptive conventions are shown to be concise and to possess straightforward mappings to hardware. The algorithms are demonstrated to be of practical complexity ($O(n^2)$, where $n$ is the number of interface events). A practical example demonstrates how the representation is used and synthesis results from five examples show that the synthesized circuitry is comparable to that achieved with other automatic methods or by experienced human designers.

References

Bisim: A Simulator for Custom ECL Circuits

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Abstract

Bisim is an event driven, transistor level, logic simulator that models both the logical and timing characteristics of custom ECL/CML circuits. Node voltages are represented by piecewise linear waveforms, transistor currents are represented by piecewise constant waveforms, and transistors are modeled as voltage controlled current switches. Bisim's realistic circuit models enable it to correctly simulate a wide variety of circuit topologies while retaining much of the speed of higher-level simulators.

References
Abstract

This paper describes XPSIM (formerly known as SuperCrystal), a multirate, event driven circuit simulator suitable for large MOS VLSI circuits. XPSIM incorporates both static and dynamic partitioning of the circuit. Each partitioned subcircuit is numerically solved with a new integration method -- the exponential function method. The voltage waveforms produced by this method are piecewise exponentials. Currently, XPSIM supports an up to third-order explicit method. Preliminary tests indicate that XPSIM exhibits a significant speedup over SPICE while retaining similar accuracy, and is able to handle large circuits.

References

A Tabular Macromodeling Approach to Fast Timing Simulation Including Parasitics

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Abstract

Most existing tabular approaches to fast timing simulation kf MOS store delay values of primitive gates as a function of output node capacitance and input slopes. These approaches, in general, do not accurately account for RC parasitic loading, overlapping inputs, and incomplete charging or discharging of output nodes. This paper presents a macromodeling approach to fast timing simulation which accounts for all of these conditions. The macromodeling splits the subcircuit into transistor gate information and loading information. In a given design many subcircuits have identical gate configurations, but each instance of a gate has a unique RC loading condition. During simulation the gate and loading information are combined and used to calculate output node voltage changes. All necessary information needed for voltage calculations are precomputed and stored in tables. Using the proposed macromodeling and the delay method greatly reduces simulation time. The approach has been implemented in a simulator called IDSIM2, and a number of large examples obtained from industry have been simulated. Speed-ups of up to three orders of magnitude have been obtained compared to standard circuit simulation, with loss of accuracy of less than 10%.

References

CMOS Inverter Delay and Other Formulas Using α-Power Law MOS Model

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Abstract

Simple yet realistic MOS model, namely [alpha]-power law MOS model, is introduced to include carrier velocity saturation effect which becomes eminent in short-channel MOSFETs. The model is an extension of Shockley's square law MOS model in the saturation region. Using the model, closed-form expressions are derived for delay, short-circuit power, and transition voltage of CMOS inverters. The resultant delay expression includes input waveform slope effects and parasitic drain/source resistance effects and can be used in simulation and/or optimization CAD tools. It is concluded that the CMOS inverter delay becomes less sensitive to the input waveform slope and short-circuit dissipation increases as MOSFETs becomes small.

References
Over-the-Cell Channel Routing

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Abstract

A common approach to the over-the-cell channel routing problem is to divide the problem into three steps: (1) routing over the cells, (2) choosing net segments, (3) routing within the channel. In this paper, we show that the first step can be reduced to the problem of finding a maximum independent set of a circle graph, and thus, can be solved optimally in \( O(n^2) \) time. Also, we show that to determine an optimal choice of net segments in the second step is NP-hard in general, and we present an efficient heuristic algorithm for this step. The third step can be done easily using a conventional channel router. Based on these theoretical results, we design an over-the-cell channel router which produces better solutions than the optimal two-layer channel routing solutions for all test examples. Our over-the-cell router also outperforms the over-the-cell router in [ShSa87]. In particular, for the famous Deutsch's Difficult Example, our solution saved 10.5% channel routing area when compared with the optimal two-layer channel routing solution, and saved 15% channel routing area when compared with the routing solution by the over-the-cell router in [ShSa87].

References

Abstract

General heuristic algorithms that have been developed in the past for channel routing, fail to fully characterize the "landscape" of nets to be routed and thus may yield sub-optimal solutions. Our track-assignment type routing algorithm makes use of an extensive set of net characteristics/relationships to perform a more "enlightened" search for an optimal routing layout than the less "informed" channel routers proposed by others in the past. When a routing problem is encountered, our algorithm resorts to subdoglegging, to a single layer segment, or to local backtracking when a solution cannot be found. Our algorithm can obtain optimal solutions for all the published channel routing examples. With some multiple cycle examples, our algorithm performs better than the public domain channel routers such as YACR2, Chameleon, or Mighty.

REFERENCES
MulCh: A Multi-Layer Channel Router Using One, Two, and Three Layer Partitions

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Abstract

Multi-layer routing is becoming an important problem in the physical design of integrated circuits as technology evolves towards several layers of metallization. Several channel routers for three layers of interconnect have been proposed, but only one, Chameleon, has been implemented to accept specification of an arbitrary number of layers. Chameleon is based on a strategy of decomposing the multi-layer problem into two and three layer problems in which one of the layers is reserved primarily for vertical wire runs and the other layer(s) for horizontal runs. In some situations, however, it is advantageous to consider also layers that allow the routing of entire nets, using both horizontal and vertical wires. MulCh is a multi-layer channel router that extends the algorithms of Chameleon in this direction. MulCh can route channels with any number of layers and automatically chooses a good assignment of wiring strategies to the different layers. In test cases, MulCh shows significant improvement over Chameleon in terms of channel width, net length, and number of vias.

References
Performance Enhancements in BOLD using "Implications"

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Abstract

In this paper, we present novel uses of "implied" network values or conditions in the context of multilevel logic synthesis. The use of these implications have resulted in performance enhanced versions, ESPRESSO_MLT2 and ML_TAUT2, of the 2 cornerstone tools of the BOLD system, ESPRESSO_MLT (Multi-level logic minimizer based on tautology checking) and ML_TAUT (Multi-level logic verifier) [2]. We first present the relationship between these "implied" values and the intermediate don't care set [3]. Then, we show how this relationship can be exploited by ESPRESSO_MLT to reduce the number of tautology calls by 50% and, more importantly, the "true" tautology calls by 80-90%. We also show how ML_TAUT2 can exploit implied network values to reduce the number of leaves in the binary recursion tree of tautology checking by as much as an order of magnitude. In addition, we discuss a parallelized version, ML_TAUT2P, of ML_TAUT2 which has attained near linear speedups on a Sun 3/75 LAN. Due to implications, ESPRESSO_MLT2, using ML_TAUT2, is expected to have speedups of up to a factor of 20 over ESPRESSO_MLT. Also, we anticipate the parallelized version of ESPRESSO_MLT using ML_TAUT2 (ESPRESSO_MLT2) to be a factor of over 100 times faster on larger problems than the previous, single processor version.

References

Don't Cares and Global Flow Analysis of Boolean Networks

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Abstract

External, intermediate, and fan-out don't care sets [1] [2] have been used to describe
information about network structure required to locally optimize a node of a boolean
network. Another method to optimize a network has been called global flow analysis [3]
[4] [5] [6]. We relate these approaches, generalize global flow to arbitrary Boolean
networks, and suggest new algorithms for these problems.

References
Sangiovanni-Vincentelli, and A. Wang "Multi-level Logic Minimization Using Implicit Don't Cares" to
appear in IEEE Trans. on CAD/ICAS.
Multiple-Level Logic Optimization System" IEEE Transactions on Computer-Aided Design, vol. CAD-6,
no. 6, Nov. 1987,
Improved Logic Optimization Using Global Flow Analysis Extended Abstract

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Abstract

This paper is concerned with techniques for automatically reducing circuit size and improving testability. In an earlier paper [2], we introduced a new method for circuit optimization based on ideas of global flow analysis. In this paper, we describe two extensions to the method. The first is a basic improvement in the primary result on which the earlier optimization was based, the second extends the applicability of the method to "conditional" optimizations as well. Together these enhancements result in improved performance for the original algorithm, as well as the ability to handle designer specified "don't cares" and redundancy removal uniformly in the framework of a graph based synthesis system such as LSS.

References

A Modified Approach to Two-Level Logic Minimization

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Abstract

The approaches to two level logic minimization can be classified into two groups: ones that use tautology for expansion of cubes and others that use the offset. Tautology based schemes are generally slow and do not obtain good expansion of cubes because of a limited global picture of the way in which the cube can be expanded. If the offset is used, usually the expansion can be done quickly and in a more global way because it is easy to see directions of expansion that do not intersect the offset. The problem with this approach is that there are many functions that have a reasonable size representation for the onset and the don't care set but the offset is unreasonably large. In this paper we present a methodology in which it is not necessary to compute the entire offset. Still a global picture is provided. This scheme has been implemented in ESPRESSO with an interface to the multilevel minimization environment MIS. Initial results show that for functions where the ratio of the size of the cover to the size of the don't care set is small, the new approach is much faster. Our initial interest was to use this mainly in a multilevel logic synthesis system where the desired don't care sets are typically large. We give some results in this environment, comparing the new scheme with ESPRESSO.

References:
CODECS: A Mixed-level Device and Circuit Simulator

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Abstract

Mixed-level device and circuit simulation allows the use of one- or two-dimensional numerical models for critical devices in a circuit configuration. CODECS is a new mixed-level device and circuit simulator that has been developed to support a variety of numerical models and analyses capabilities. Effective coupling of device and circuit simulation capabilities is achieved by a proper choice of algorithms and architecture. Several examples illustrate the advantages of CODECS for simulating both MOS and bipolar circuits.

References
A Grid Generation System for Process and Device Simulation

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ABSTRACT

A new method is presented for numerically generating boundary-fitted coordinate systems for arbitrarily shaped three dimensional regions such as LOCOS (Local Oxidation of Silicon) isolation regions, Trench Cells, or Stacked Capacitor Cells for next-generation DRAM. In this method, the three dimensional region of interest is decomposed into curve-bounded surfaces which are free-form surfaces with spline curves defining the surfaces. Grid points for the surfaces are generated by the boundary-fitted coordinate method which improves convergence and accuracy.

The usefulness of this system is illustrated through a series of examples and applications in the semiconductor process and device simulation.

REFERENCES

A Submicron MOSFET Model for Simulation of Analog Circuits

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Abstract

This paper provides an efficient MOSFET model for accurate prediction of the drain current and the drain conductance of a short-channel MOSFET. Earlier models for channel length modulation are not suitable for simulating analog circuits where the drain conductance is important. Empirical expressions derived from measured I-V characteristics are used to fit the observed behavior of drain conductance with gate and substrate bias. None of the models currently used for circuit simulation predict the effects of gate and substrate bias adequately. Results on the use of this new model in analog circuit simulation are presented.

References
ABSTRACT

This paper presents a generalized precise and computer efficient table look-up model applicable to MOSFETs, MESFETs, and BJTs. The model has been optimized and implemented into SPICE 2G.6 for analog large signal and small signal applications. The local and global accuracy is adjustable to within the limits of process variation. This model has been applied in spice circuit simulator to predict the DC and AC performance of complex analog circuits such as a 1 µm op amp more accurately and efficiently than conventional analytical models. The memory requirement for the model is 432 data points, which is less than 10 kbytes.

REFERENCES

Gate Matrix Partitioning

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Abstract

An heuristic gate matrix partition algorithm is presented. It partitions a gate matrix into two matrices such that the total area and the aspect ratio of the circumscribing rectangle are improved. The algorithm is based on the min-cut algorithm [4] [5]. The gain function and balance condition are redefined for the gate matrix problem. The time complexity of the algorithm is \(O(t) + O(n|G_{sub.L}||LB)\), where \(t_i\) is the number of transistors, \(n\) the number of nets, \(|G_{sub.L}||LB\) the number of long gates, and \(LB\) the maximum number of nets on a gate. Experimental results show significant improvement over the layout without partition. For the three examples of a previous paper the area reduction ranges from 20% to 30%. The aspect ratio improves from 2.59, 2.63, and 4.00 to 1.11, 1.16, and 1.18, respectively.

References

Doubly Folded Transistor Matrix Layout

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ABSTRACT

We present a flexible module generator that lays out transistor net lists. New is the formulation of this layout problem as a two-dimensional folding problem. The folding algorithm uses an elegant hierarchical divide and conquer technique. The aspect ratio and pin positions can be controlled within a wide range, while the area remains approximately constant. Accurate control of the aspect ratio and pin positions is important in combination with top-down floor planning. The mask generator uses a small library of adaptable transistors with parameters like length, width, positions of the terminals, and an optional diffusion implant. Compared to other automated layout styles, the new module generator makes smaller and more flexible layouts. The layout of the modules can be customized with respect to all major design parameters: function, speed, design rules, aspect ratio and pin positions.

REFERENCES

ABSTRACT

Efficient algorithms for CMOS gate matrix layouts are presented, which have fully utilized the duality between NMOS and PMOS. Improper assumptions made by previous works are pointed out. Problems which have prevented previous algorithms from reaching a real optimal result are discussed and solved. Significant improvements are achieved over previous algorithms.

References

CLAY: A Malleable-cell Multi-cell Transistor Matrix Approach for CMOS Layout Synthesis

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ABSTRACT

CLAY takes a netlist partitioned down to the transistor level, a technology file with an arbitrary number of metal layers, and constraints on aspect and IO signal positions to produce mask geometries. CLAY attempts to capture in software layout knowledge at the transistor level (allowing variable shaped cells including heights) and at the floorplan level for VLSI sized examples. CLAY compares well against standard cell and manual approaches.

REFERENCES

Decomposition and Factorization of Sequential Finite State Machines

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Abstract

In this paper, we present algorithms for decomposing a finite state machine into smaller interacting machines so as to optimize area and performance of the eventual logic implementation.

Cascade decomposition algorithms, which decompose a given machine into an independent and dependent component, have been proposed in the past. However, good cascade decompositions rarely exist in modern finite state machine designs. We propose a more powerful form of decomposition where both components of the decomposed machine interact with each other. This form of decomposition involves identifying subroutines or factors in the original machine, extracting these factors and representing them as a separate factoring machine. The occurrences of these factors become calls to the factoring machine from the factored machine.

Given a State Transition Graph description of a machine, we have developed algorithms which can identify factors in the machine that produce good decompositions. Experimental results indicate that this factoring technique for state machine decomposition is superior to cascade decomposition techniques.

References
A Fast Algorithm for the Optimal State Assignment of Large Finite State Machines

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Abstract

Most of the recent state assignment procedures are tightly coupled to specific combinational logic synthesis algorithms. These logic synthesis algorithms are fairly complex and to a large extent determine the complexity of the assignment procedure. We present a state assignment procedure that uses only abstract complexity criteria and produces assignments that are not targeted towards particular implementations. It produces networks similar in complexity to those obtained by contemporary methods but is an order of magnitude faster.

References

A New Method for the Efficient State-Assignment of PLA-Based Sequential Machines

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ABSTRACT

A new method for the state assignment of Finite Sequential Machines is proposed. The new algorithm gives solutions with a minimum number of state variables instead of with minimal-cardinality next-state functions. Comparisons between the results given by our method and other previously reported have shown a clear superiority of the new algorithm in terms of silicon area, specially for big machines.

REFERENCES

Critical Path Tracing in Sequential Circuits

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Abstract

Critical path tracing in an alternative to fault simulation for combinational circuits. The method has been shown to be faster than traditional fault simulation methods, but produces pessimistic results in some cases involving reconvergent fanout.

In this paper, we extend critical path tracing to synchronous sequential circuits. We first show that the pessimistic nature of critical path tracing in combinational circuits may lead to incorrect results that are not necessarily pessimistic in sequential circuits. We then propose a modification of the method for removing the approximation, and then present the critical path tracing algorithm for synchronous sequential circuits.

References

A Fast Fault Simulation Algorithm for Combinational Circuits

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ABSTRACT

The performance of a fast fault simulation algorithm for combinational circuits, such as the critical path tracing method, is determined primarily by the efficiency with which it can deduce the detectability of stem faults (stem analysis). We propose a graph based approach to perform stem analysis. A dynamic data structure, called the criticality constraint graph, is used during the backward pass to carry information related to self masking and multiple-path sensitization of stem faults. The structure is updated in such a way that when stems are reached their criticality can be found by looking at the criticality constraints on their fanout branches. Compared to the critical path tracing method, our algorithm is exact and does not require forward propagation of individual stem faults. Several examples are given to illustrate the power of the algorithm. Preliminary data on an implementation is also provided.

References
A Fault Simulation Method Based on Stem Regions

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Abstract

We have used the concept of stem regions as a framework for a fast fault simulator for combinational circuits. The concept allows a static reduction of the circuit area of explicit analysis, for single as well as multiple output circuits. A dynamic reduction of processing steps is also achieved as the fault simulation progresses and fault coverage increases. Both the static and dynamic reductions are fully compatible with the parallel pattern evaluation technique, resulting in a very efficient implementation. The simulation algorithm is described, and experimental results are shown for the well known benchmark circuits.

References

A New Algorithm for Standard Cell Global Routing

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Abstract

In this paper, we present a new algorithm for standard cell global routing. The algorithm considers all of the interconnection nets in parallel; this produces superior results since information about all of the nets is available throughout the global routing process. We formulate the global routing as finding the optimal spanning forest (a generalization of optimal spanning trees) on a graph that contains all of the interconnection information. The results of several theorems allow us to prune many non-optimal connections before the process begins. This approach successfully solves the net ordering and congestion prediction problems which other approaches suffer. The new algorithm was implemented as part of the DATools system at Xerox PARC. The benchmarks from the Physical Design Workshop are used as part of the comparison suite. The new algorithm achieves up to 11% area reduction compared to the previous global routing package used in the DATools system and obtains up to 17% reduction in the total channel density compared to the Timberwolf 4.2 package. In no case does the new algorithm do worse than its competitors.

References

A New Global Router for Row-Based Layout

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Abstract

We have developed a new global router for row-based layout styles such as sea-of-gates, gate array, and standard cell circuits. The new global router is part of the latest version of TimberWolfSC, a placement and routing package for row-based layout. Our algorithm outperformed the UTMC Highland system on two standard benchmark circuits. Furthermore, in tests on ten circuits, the new global router produced track counts which were an average of 27 percent lower than the previous TimberWolfSC global router. The new global router is an average of 30 times faster than the previous algorithm. Our new global router has been generalized to handle macro blocks on the chip, equivalent sets of pins, single pins (those without an equivalent), and circuits having many or no built-into-the-cell feeds. Indiscriminate over the cell routing is also handled.

References

[10] The UTMC Highland system results for the primary 1 and primary 2 benchmark circuits were run and reported by Ken Roberts, then at UTMC. The results were published in a memo entitled "Place-Off Participant Results from Ken Roberts, 6-16-87."
Channel Routing Order for Building-block Layout with Rectilinear Modules

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Abstract

In this paper we present a feasible channel ordering algorithm for building-block layout consisting of rectilinear blocks. Existing approaches for layout with rectangular modules using only straight and L-shaped channels are no longer applicable. An important class of channels called monotone channel is introduced. Our algorithm produces a feasible channel order which minimizes the number of non-monotone channels and the maximum number of corners in a channel used.

References
Abstract

Current techniques in logic/fault simulation treat the problem as a non-numeric one in which the basic primitives involved are Boolean operations, string matching/manipulation operations, bit-or word-wise comparison operations, etc. This paper describes a novel technique for reformulating the problem in terms of standard vector and matrix operation primitives which are well-supported on all scientific machines. For the purposes of this paper, the overall computing environment is assumed to be a scientific/engineering one, with Fortran as the primary coding medium and the hardware biased toward numerically intensive applications. Also, we restrict our attention to VLSI array logic.

References

Parallel PLA Fault Simulation Based on Boolean Vector Operations

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Abstract

An efficient PLA crosspoint fault simulation algorithm is presented. Parallel Boolean vector operations on a bitwise representation of PLA faults replace set operations, leading to increasing efficiency as PLA size grows. Experimental results demonstrate execution times averaging over 100% faster than PLATYPUS and almost two and a half orders of magnitude faster than the CHIEFS fault simulator.

Keywords: Crosspoint fault Model, Fault simulation, PLA testing

References
Abstract

The accessibility of vector processors through computer networks makes them excellent candidates for accelerating fault simulation of VLSI circuits. In this paper, a highly vectorized parallel fault simulation (VPFS) algorithm developed to take advantage of the specific hardware architecture of the Cray X-MP is described. The data structure is optimized to suit the constraints imposed by the design of the main memory on the Cray supercomputer. The implementation of VPFS on a Cray X-MP/24 achieved a peak performance of about $2.5 \times 10^{9}$ gate-evaluations per second on one processor, for a maximal speed-up of PI over scalar processing.

References

CREST - A Current Estimator for CMOS Circuits

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ABSTRACT

CREST is a pattern-independent current estimation approach developed to support electromigration analysis tools. It uses the powerful, original concept of probabilistic simulation to efficiently generate accurate estimates of the expected current waveforms. As originally implemented, CREST was restricted to circuits with no pass transistors and no reconvergent fanout or feedback. This paper extends the approach to circuits containing pass transistors, reconvergent fanout, and feedback, and provides heuristics to efficiently simulate circuits with large reconvergent fanout or feedback blocks. The results of CREST on several real circuits are presented.

REFERENCES

ABSTRACT

A time-domain current waveform simulator for the power buses of CMOS circuits is presented. The simulated waveform, instead of the average estimation, helps solving the VLSI reliability problems due to the electromigration and excessive voltage drops in the power bus. Based on the event-driven technique and the precharacterized switch-level delay model, the simulator can handle circuits as large as $10^3 \sim 10^4$ transistors in $10^1 \sim 10^2$ CPU seconds on the Sun-3 workstation. The simulated waveform in worst cases may only deviate 20% from those computed by SPICE.

REFERENCES

Current Estimation in MOS IC Logic Circuits

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ABSTRACT

This paper deals with estimating currents in nMOS/CMOS IC logic circuits at the gate level and macro level. The estimates are to be used for reliable design of power and ground buses. An accurate and efficient model of a gate is used to develop algorithms to estimate the maximum currents. The algorithms provide trade-off between run time and the quality of solution. Experimental results are included.

REFERENCES

Combining Circuit Level Changes with Electrical Optimization

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ABSTRACT

A difficult task for VLSI designers is to produce layout which satisfies electrical performance and area requirements. We have developed a program, called EPOXY, which sizes a circuit’s transistors to satisfy performance and area constraints. If these cannot be met, the program considers small circuit changes in an effort to meet the constraints. The changes it considers include inserting buffers, replicating logic, splitting large transistors and reordering transistor trees are evaluating using this system. Several CMOS examples demonstrate how EPOXY applies these heuristics to meet difficult timing constraints, power requirements, and cell width and height limitations. Compact layout and aspect ratio requirements are handled by a virtual grid area model. From an implementation viewpoint, EPOXY’s underlying equation abstraction of circuit performance automatically provides critical path information and allows rapid modification of the circuit structure. When applied to a CMOS 16-bit adder, a speed improvement of 23% was achieved over transistor sizing alone while satisfying a height constraint. Similarly, the speed of a dynamic CMOS PLA was improvement by 10% and an array of CMOS JK flip-flops by 23%.

References
A Method for Net Representation with Polygon Decomposition

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Abstract

This paper presents a method of decomposing polygons into convex sub-polygons. The result gives accurate polygon areas and maintains the tree structure relationships of net branches represented by the polygon. Contacts which connect polygons on different layers are used. The whole net can be represented in a backward linklist. Signal delay in RC tree network [6] has been implemented into this algorithm.

References:
ABSTRACT

NOISY is part of an Electrical Rule Checker with original emphasis on noise computation. NOISY analyses all types of noise, computes worst-case conditions using a relaxation algorithm, and draws a map of noise distribution in a chip. Its hierarchical organisation allows verification of a high complexity chip (more than 100,000 transistors). Developed for CMOS circuitry, both static and dynamic, it can be extended to other types of technology.

State of the Art CAD tools offer sophisticated verification of functional behaviour for Ultra-Large-Scale-Integrated Circuits, but provide poor capabilities for electrical checking. They are often limited to verification of topological rules, ignoring noise problems. Noise is defined as all parasitic spikes, super imposed to nominal signals. With CMOS technologies, which generate very sharp current pulses, this problem has become more and more critical with increasing integration density. So, an efficient control of noise is mandatory for "First-Run-Silicon".
Aliasing Probability of Non-Exhaustive Randomized Syndrome Tests

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Abstract

A comprehensive design methodology which includes built-in self-test (BIST) cannot be achieved without performance measures of BIST techniques. This paper derives exact and asymptotic expressions for the aliasing probability of randomized syndrome testing using the independent error model recently proposed by Williams et al. It is shown that randomized syndrome testing outperforms signature analysis for a substantial class of functions, and that existing methods may be used to transform the remaining functions during test mode.

References
Built-In Self-Test for Large Embedded CMOS Folded PLAs

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Abstract

There are a number of Built-In Self-Test (BIST) design methods proposed in the literature for PLAs. None of these methods addresses the applicability to folded PLAs. In this paper we present the first known BIST design method for large embedded CMOS folded PLAs. This method requires about half the testing time and comparable area overhead of deterministic BIST methods applied to corresponding non-folded PLAs. We give tests to detect stuck-at, bridging, cross-point and stuck-open faults.

References

On the Design of Robust Multiple Fault Testable CMOS Combinational Logic Circuits

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ABSTRACT

It is known that circuit delays and timing skews in input changes influence choice of tests to detect delay faults. Tests for stuck-open faults in CMOS logic circuits could also be invalidated by circuit delays and timing skews in input changes. Tests that detect modeled faults independent of the delays in the circuit under test are called robust tests. An integrated approach to the design of combinational logic circuits in which all single stuck-open faults and path delay faults are detectable by robust tests was presented by the authors earlier. This paper considers design of CMOS combinational logic circuits in which all multiple stuck-at, stuck-open and all multiple path delay faults are robustly testable.

REFERENCES

CHAMP: Concurrent Hierarchical And Multilevel Program for Simulation of VLSI Circuits

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ABSTRACT

This paper discusses the design and implementation of a hierarchical switch-level simulator for complex digital circuits. The hierarchy is exploited to reduce the memory requirements of the simulation, thus allowing the simulation of circuits that are too large to simulate at the flat level. The algorithm used in the simulator operates directly on the hierarchical circuit description. Speedup is obtained through the use of high level models. The simulator is implemented on a SUN workstation and has been used to simulate a switch level description of the Motorola 68000 microprocessor.

References


The Logic Automaton Approach to Accurate and Efficient Gate and Functional Level Simulation

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Abstract

Applying a mathematical formalism to event-driven simulation has led to model correctness and highly efficient implementation. MSI functional models with accurate delays are compiled into transition tables of elementary state-machines that are interconnected to model networks. Simulation consists to compute the state trajectories of these machines, using the generated state transition tables.

References

Simulating Mixed Analog-Digital Circuits on a Digital Simulator

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ABSTRACT

Time domain simulation of circuits which contain analog functional blocks such as gain stages, filters, and analog-digital conversion modules can be concurrently simulated with digital components on an event driven digital simulator. A technique for modeling such analog circuits as "digital" behavior models has been developed and simulation of mixed analog-digital circuits based on this methodology has been implemented at Gould on an accelerated digital simulator. An automatic gain control circuit is presented as an example.

REFERENCES

M³ - A Multi-Level Mixed-Mode Mixed D/A Simulator

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ABSTRACT

This paper describes M³, a unified multi-level mixed-mode simulator for mixed digital-analog circuits. The methodology allows digital, analog and mixed D/A portions of the circuit to be described at various levels ranging from behavioral, functional, cell, to transistor level. While the analog portions of the circuit are simulated with maximum accuracy, the digital portions can be simulated in various modes. M³ is event driven and uses block elimination with unique reordering and pivoting techniques to accommodate state variables for behavioral analog or mixed D/A models. The simulator has been integrated into the MOTIS3 design verification system. A representative mixed D/A simulation example is included.

REFERENCES

Modeling and Enhancing Virtual Memory Performance in Logic Simulation

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ABSTRACT

To achieve acceptable performance, virtual memory systems generally rely on the presence of a high degree of spatial and temporal reference locality during code execution. The enormous quantity of intricately related data typically found in logic simulation makes this a dubious assumption. There simply is no way to statically organize circuit representation data to ensure locality. This phenomenon is explored through the analysis of address reference data obtained from a logic tester monitoring simulation execution on a general-purpose virtual memory workstation. Data from code compilation runs are included to illustrate the differences in reference behavior found between logic simulation and more conventional applications. An improved virtual memory management scheme based on speculative references and tuned to logic simulation is presented.

REFERENCES

Logic Simulation on Vector Processors

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Abstract

We compare the performance of three commercial vector computers, viz., the Cray X-MP/48, IBM 3090/400, and Alliant FX/8, for simulating logic circuits at the gate level. Our experiments that assume zero- and unit-delay models demonstrate that certain key architectural features, in particular, the presence of a scalar cache, have an adverse impact on the potential speedup. Consequently, the achievable speedup due to vectorization of simulation code, while still substantial, is less than what others have reported. Our results indicate that concurrent operation of multiple CPUs in vector mode in machines such as the Alliant FX/8 may be the most cost-effective speedup technique for logic simulation on current vector processors.

References
Discrete-Event Simulation on Hypercube Architectures

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Abstract

This paper presents a performance model of a hierarchical discrete-event simulation algorithm running on a hypercube architecture. We assume a static allocation of system components to hypercube processors and a global clock algorithm with an event-based time increment. Following development of the performance model, it is applied to a digital systems simulation application. The effects of different architectures, algorithm parameter values, and partitioning strategies on speedup are evaluated.

References
Parallel Polygon Operations Using Loosely Coupled Workstations

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Abstract

Problems in two dimensions, such as the polygon operations which are performed on IC designs prior to fabrication, lend themselves well to functional distribution. We present a method for performing polygon operations in parallel which utilises distributed workstations, obviating the need for performance improvement by special-purpose hardware. The method provides improved performance while remaining cost effective and flexible. As designs become larger more computers can be incorporated into the network. Results are presented for runs on collections of proprietary workstations.

References

Timing Optimization of Combinational Logic

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Abstract

We present an algorithm for speeding up combinational logic with minimal area increase. A static timing analyzer is used to identify the critical paths. Then, a weighted min-cut algorithm is used to determine the subset of nodes to be resynthesized. This subset is selected so that the speed-up is achieved with minimal area increase. Resynthesis is done by selectively collapsing the logic along the critical paths, and then decomposing the collapsed nodes to minimize the critical delay. This process is iterated until either the timing requirements are satisfied or no further improvement can be made. The algorithm has been implemented and tested on many design examples with promising results.

References
Experiments in Logic Optimization

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Abstract

We have conducted a number of experiments, gathering over 5000 data points, to answer several important questions about logic optimization and its application to high-level synthesis. Our experiments, synopsized in this paper, show that: logic optimization is competitive in area with manual design; stronger optimization methods give somewhat better average results (10% - 30%) at much greater computational cost (8X and more); fast logic optimization methods can be used to estimate the average results of the more powerful, costly methods; and literal count is a good estimator of area before routing for standard cell designs.

References
Boolean Decomposition in Multi-Level Logic Optimization

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Abstract

In this paper, we propose multiple-valued Boolean minimization as a technique for identifying and extracting good Boolean factors which can be used as strong divisors to minimize the literal count and the area of a multi-level logic network.

Given a two-level logic function, a subset of inputs to the function is selected such that the number of good Boolean factors contained in this subset of inputs is large. In previous work, we developed a selection algorithm based on an estimation of the multiple-valued cover cardinality obtained by representing all combinations of the selected inputs by a single multiple-valued variable. If the targeted implementation is a set of interconnected PLA’s, the different cube combinations given by this subset of inputs are re-encoded to reduce the number of product terms in the logic function. The re-encoding process incorporates a new encoding algorithm, superior to previous techniques, which minimizes the number of product terms in the re-encoded logic function given a constraint on the number of bits to be used. When targeting a general multi-level network, we are concerned with minimizing the literal count of the network. We have developed new algorithms that identify a set of factors which maximally decrease the literal count of the logic network when used as strong divisors.

We present results obtained on several benchmark examples that illustrate the efficacy of our techniques.

References

Hill Climbing with Reduced Search Space

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Abstract

We present a general optimization algorithm, which in some areas successfully competes with simulated annealing, the Kernighan-Lin algorithm, as well as special heuristics. It gains speed by taking advantage of the structure of the objective function in order to reduce the search space.

References

ABSTRACT

A decomposition technique known as Node Tearing could be used to perform Circuit Simulation on a multiprocessor. This paper deals mainly with the effect of partitioning the circuit (i.e., the choice of tearing nodes) on the final speedup achieved. Using a very simple model for the LU decomposition time of sparse matrices, a circuit partitioning problem, based on node tearing, is formulated such that the resulting speedup on a multiprocessor (assuming enough processors are available) is a maximum. An abstract hypergraph partitioning problem is then posed along with an algorithm for its solution. Finally, the original circuit partitioning problem is transformed into an equivalent hypergraph partitioning problem, thereby generating partitions for the circuit. The algorithm developed, however, partitions the circuit into only two (balanced) parts. To generate more parts the algorithm is simply used recursively. The tradeoff in circuit partitioning time versus the number of available processors on the speedup factor is also studied.

REFERENCES

iPRIDE: A Parallel Integrated Circuit Simulator Using Direct Method

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ABSTRACT

This paper describes a parallel circuit simulator, iPRIDE, which uses a direct solution method and runs on a shared memory multiprocessor computer. The simulator is based on a multilevel node tearing approach which produces a nested bordered-block-diagonal (BBD) form of the circuit equation matrix. Parallel solution of this nested BBD matrix will be described. The efficiency of this parallel solution will be shown to depend on how the circuit is partitioned as well as the sequence the concurrent tasks (scheduling) is solved. A partitioning heuristic is first proposed assuming arbitrary number of processors available. Scheduling methods are studied when the number of processors is fixed. The optimal level of partitioning depends on the number of processors as well as the scheduling methods. A method of determining this optimal level will also be described. The program is implemented on an ALLIANT FX/8 multiprocessor with shared memory. The performances of the program will also be given.

REFERENCES


A Band Relaxation Algorithm for Reliable and Parallelizable Circuit Simulation

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ABSTRACT

A variable-band relaxation algorithm for solving large linear systems is developed as an alternative to Gauss-Jacobi relaxation. This algorithm seeks to improve the reliability of Gauss-Jacobi relaxation by extracting a variable-sized band from the matrix and solving that band directly. This leads to a relaxation algorithm with provably better convergence properties. Furthermore, this algorithm can be used effectively on a massively parallel computer, because band matrices can be solved in \( \log(n) \) time on PI which compares the convergence properties of variable-band relaxation to Gauss-Jacobi relaxation.

References


Taking Advantage of Optimal On-Chip Parallelism for Parallel Discrete Event Simulation

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Abstract

It is impossible to get more than some optimal level of performance from parallel discrete event simulation. The optimal depends on several factors: the circuit being simulated, the vectors being simulated and the machine upon which the simulation is being performed. Recent empirical studies based upon very simple models suggest that the amount of parallelism available in typical circuits is very small. We present a new model of optimal performance for a machine with an infinite number of processors having uniform memory accesses. The model demonstrates that some circuits have significantly more parallelism than previously believed. The model is refined to define the optimal load partitioning for a machine with a finite number of processors with uniform access. We extend the model to define the optimal static data partitioning. Using these models, a metric is obtainable which can be used to benchmark different models of parallel simulation. We show the effectiveness of these models in detecting performance problems of our version of RSIM running on BBN's Butterfly.

References

ABSTRACT

A stick diagram extraction program SKELETON has been developed to make use of past handcrafted layout, which is valuable property, in symbolic layout system. It transforms a physical layout into an equivalent stick diagram. Centralized terminals and dispersed terminals are proposed for the spacing program without adaptability to the change of design rules. A heuristic procedure is presented to reduce jogs.

REFERENCES

GeminiII: A Second Generation Layout Validation Program

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ABSTRACT

Gemini is a circuit comparison program that is widely used to compare circuit layout against a specification. In this paper we describe recent extensions made to Gemini that make it faster, enable it to isolate errors better, and extend its domain of application. This has been done by changes to the labeling algorithm, extensions to the local matching algorithm, better handling of symmetrical circuits and the accommodation of series-connected transistors. GeminiII's algorithm is separated into global labeling and local matching phases. GeminiII dynamically switches between the two depending on the amount of local structure contained in the circuit, taking advantage of the speed of the local matching algorithm when possible and relying on the power of the more general algorithm when the simple algorithm fails. This blending of algorithms also allows differences between two circuits to be better contained so that defects can be pinpointed.

References
PACE: A Parallel VLSI Extractor on the Intel Hypercube Multiprocessor

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ABSTRACT

Hypercube multiprocessors have recently offered a cost-effective and feasible approach to supercomputing by directly connecting a large number of low-cost processors with local memory, which cooperate on tasks by message-passing instead of shared variables. In this paper, we propose an efficient parallel algorithm to speed up the VLSI circuit extraction task on a hypercube multiprocessor. The basic approach used in our parallel circuit extractor is the partitioning of a circuit into smaller regions, assigning each region to a processor of the hypercube, and having the processors cooperate in performing the extraction procedures. The proposed algorithm is sufficiently general so as to support the use of different models for electrical parameter calculations of varying degrees of accuracy and computational complexity. The parallel algorithm has been implemented in a program called PACE (PArallel Circuit Extractor) on the Intel iPSC/D4-MX hypercube. Results of the speedups of the algorithm on many realistic VLSI circuits are presented.

REFERENCES
An Efficient Sequential Range Query Model for Minimum Width/Space Verification

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ABSTRACT

A new algorithm is presented which efficiently reports minimum width/space violation in a geometric mask pattern. The proposed algorithm solves a sequence of range search problems by employing a plane sweep method. The algorithm runs in $O(n \log n)$ time, which is theoretically optimal. It requires $O(n^{0.5})$ space which is very efficient in practice. Moreover, this algorithm, we believe, is easy to implement and practically fast (116.7 seconds for a rectilinear region with $2.5 \times 10^5$ vertices on VAX 8650).

References
In this paper we present a formal methodology for IC performance testing, called predictive subset testing, that is based upon a statistical model of parametric process variation. In this Monte Carlo approach, we use a statistical process simulation, coupled with circuit simulation, to determine the joint probability distribution of a set of circuit performances. By evaluating the joint probability distribution, rather than assuming the performances to be independent, we are able to exploit correlations that exist between them and reduce the number of performances that need to be explicitly tested. Once a subset of performances for explicit testing has been identified, we construct regression models for the untested performances, and from the confidence intervals, assign test limits for the tested performances. In this manner, we can predict the values of the untested performances within desired quality levels, reducing test complexity and cost.

References
Built-In Current Testing - Feasibility Study

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Abstract

A testing methodology which applies built-in current sensors to detect abnormal currents in the power buses of functional blocks of CMOS ICs may be used to significantly improve the test quality of VLSI circuits. This paper proposes Built-In Current (BIC) testing in which appropriately derived testing vectors and built-in current sensors are applied. Simulation results and design experiments are summarized in order to demonstrate the feasibility and to illustrate the applicability of this approach. Demonstrated results suggest that Built-In Current testing may be a very powerful tool for overcoming basic bottlenecks in VLSI testing. It may provide very inexpensive testing, high quality built-in testing, or on-chip concurrent reliability testing for high quality fault tolerant systems.

References
Testing Oriented Analysis of CMOS ICs With Opens

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Abstract

In a typical approach to VLSI testing opens are modeled by the "transistor stuck-open" fault model or are not explicitly covered at all. This paper demonstrates that functional faults caused by opens, i.e. by regions with missing material, cannot be modeled well by a transistor stuck-open. It also shows that the majority of opens which occur in CMOS static circuits manifest themselves as timing faults. The analysis of the behavior of a MOS transistor with a floating gate indicates it acts as a weakly "on" active load, and therefore an open gate cannot be detected by stuck-fault testing but may be detected by monitoring the static current through the power buses.

REFERENCES
Automatic Modeling of Switch-Level Networks Using Partial Orders

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Abstract.

A key idea in switch-level simulation is the use of a total ordering of signal strengths to resolve conflicts between opposing signals. For many circuits, however, it is not possible to assign such strengths to circuit elements in a logically consistent fashion without user intervention. We show that the use of a partial ordering of strengths avoids these difficulties and allows modeling to be done automatically. The problem of minimizing the number of distinct strengths needed to model a circuit is also discussed because simulation times are affected by the number of strengths being used. This is especially important for compiled switch-level simulators that generate representations whose size is proportional to the number of strengths. Statistics are presented on the application of these ideas to industrial chips.

References.
Data Parallel Switch-Level Simulation

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Abstract

Data parallel simulation involves simulating the behavior of a circuit over a number of test sequences simultaneously. Compared to other parallel simulation techniques, data parallel simulation requires less overhead for synchronization and communication, and it permits higher degrees of parallelism.

We have implemented two data parallel versions of the switch-level simulator COSMOS. The first runs on conventional machines, exploiting the bit parallelism of machine-level logic operations. This version runs 20-30 times faster than sequential simulation on the same machine. The second runs on a massively-parallel SIMD machine, with each processor simulating the circuit behavior for a single test sequence. The simulator running on a 32,768 processor machine runs up to 33,000 times faster than sequential simulation on a workstation computer.

References
Abstract

Various novel algorithmic and heuristic techniques are proposed for dealing with the problem of computing delays in switch-level models of MOS transistor circuits which contain loops. The nonlinear dependence of the effective channel resistance on the capacitive load is dealt with by adjusting the resistance within the iterative process of computing delay, based on the Lin and Mead algorithm. Heuristics are proposed for reducing the number of iterations by splitting the loops at high capacitance nodes and by assigning the initial values of the split capacitances on the basis of path conductances. It is demonstrated that the decomposition of the transistor groups into bicomponents is a very effective technique in large groups. Combinations of these techniques have been tested on a large variety of circuits, a representative subset of which is presented here.

References

Optimal CMOS Cell Transistor Placement: A Relaxation Approach

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Abstract

We describe a relaxation approach for producing a placement of transistors in a CMOS cell in a grid layout style directly from the circuit schematic diagram. For a given objective function, the approach leads to optimal results in most of the cases attempted. Unlike previous constructive approaches, our approach is iterative. Earlier work often concentrated exclusively on row width minimization by maximal sharing of diffusion among adjacent transistors. We show that our procedure is quite flexible and can be used to solve unrestricted circuit types, and for a variety of other important parameters affecting the wirability of layout. The procedure is targeted for use in the automatic generation of custom and gate-array cell libraries.

References
A New Layout Optimization Methodology for CMOS Complex Gates

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ABSTRACT

Efficient algorithms for the layout generations of CMOS complex gates are presented. Heuristics which use the concept of delayed binding are introduced. An optimized net list is decided during the layout generation phase (instead of before the layout generation). Results of examples show that this new approach can achieve a considerable improvement over previous ones.

References
iCOACH: A Circuit Optimization Aid for CMOS High-Performance Circuits

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ABSTRACT

iCOACH is a two-pass iterative circuit optimizer which generates a polycell-based layout from a gate-level description file and user-defined timing constraints. The first pass is to place and route the cells and extract the interconnection parameters. The second pass optimizes the circuit at the transistor level and makes necessary pitch-matchings. Although iCOACH has the layout style similar to the polycell approach, it is distinct in two important aspects. First, iCOACH does not rely on any fixed cell library. Instead iCOACH generates customized cells by invoking the circuit optimizer and performs the transistor-level optimization for both static and dynamic CMOS circuits. Secondly, although the cells in the same row are required to have the same height, different rows can have different heights to make circuit more compact. Dynamic circuits are used with a careful treatment on reliability issues related to charge sharing and noise margin. A novel polycell layout style is introduced for dynamic CMOS circuits. A 4-bit ALU and a 32-bit adder examples are presented to demonstrate the capability of iCOACH.

REFERENCES

An Efficient Compaction Algorithm for Test Vectors of Microprocessors and Microcontrollers

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Abstract

Test vectors are commonly derived from logic simulation output. If the entire test program would not fit into the target VLSI tester's memory, test vectors must be compacted. Otherwise, more than one load of the tester memory would be necessary, increasing the production test time and cost. A new compaction algorithm for test vectors of microprocessors and microcontrollers is presented. It takes advantage of the fact that repeating patterns in the simulation output of microprocessors and microcontrollers occur due to specific reasons. An instance of each different multiply occurring repeating pattern is extracted as a subroutine in an efficient manner, as compared to ad hoc approaches used earlier. Compaction is then achieved by replacing the repeating patterns by calls to appropriate subroutines. The algorithm has been implemented in a "C" program and excellent results obtained, which are discussed.

References

Compaction of ATPG-Generated Test Sequences for Sequential Circuits

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Abstract

Currently available Automatic Test Pattern Generators (ATPGs) generate test sets that are non-optimal in length. Since the cost of testing depends on the length of the test set, previous researchers reduced the test length by applying compaction techniques. These techniques were directed towards combinational circuits and are not directly applicable to sequential circuits because the test sequences must maintain a strict ordering of the patterns. This paper describes a number of new heuristic techniques to reduce the length of the test set for a sequential circuit by compaction of the sequences generated by an ATPG. Based on these techniques, a program has been written in C that achieved 56%-73% reduction in test length of a highly sequential circuit obtained from industry.

References

Efficient Handling of Large Wiring Data in TANGATE

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Advances in VLSI have made possible gate array designs containing over 100K used gates, as large as 50K objects and 50K nets. These large designs challenge the CAD database designer to support fast access to all information necessary for the physical layout of the chip while staying within restricted memory and disc space.

The TANGATE database was specifically designed with these needs in mind. A new, hierarchical wiring structure has resulted in an extremely compact representation for detailed routing information. Interfaces to support geometric searching have resulted in good performance despite the overhead of unpacking the wiring data, and form the basis for many TANGATE algorithms.

References
Abstract

Cbase 1.0 is a multilayered system which provides a common repository of both VLSI objects and their associated operations, a tool interface for writing new applications, and a user interface for invoking applications or viewing objects in the database. Our preliminary experience indicates that using an Object-Oriented database provides features such as specialization/generalization, property and operation inheritance, and polymorphism among object types, which are useful for modeling the hierarchical nature and multiple views of a circuit.

References

Flexible Module Generation In The FACE Design Environment

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ABSTRACT

The Flexible Architecture Compilation Environment (FACE) provides a common object-oriented representation for design information. This paper discusses a module generation system built within the FACE environment that uses parameterized procedural module descriptions. These generators capture the knowledge of a designer and facilitate a high level of reuse of the modules and leaf cells. The system provides a general mechanism to parameterize design information and supports complex generators ranging from tiled structures to entire chips. This approach is applicable to many hardware architectures, and we discuss observations from designing working VLSI chips.

REFERENCES
Abstract

We consider the problem of finding the minimum-length rectilinear Steiner tree that connects a set of points on the boundary of a rectangle. We present a linear time algorithm for this problem.

References

Topological Channel Routing

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Abstract

We present a new approach to two-layer channel routing using a new layout model which utilizes the channel area more efficiently than the traditional layout model. Our unique model allows horizontal and vertical wire segments to be placed on both layers while avoiding the cross talk problem. In order to have as many nets without vias as possible, the crossing relationship among the nets is determined before they are mapped onto a channel. Preliminary experimental results are very encouraging.

References

A New Algorithm for Topological Routing and Via Minimization

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Abstract

A new topological routing method is presented for the two layer routing of printed circuit boards and VLSI chips. The primary criterion to the topological routing in this paper is via minimization. We allow multi-terminal nets and multiple wires to intersect at any via. After topological routing, the via minimization problem is then formulated as a \{0, 1\} linear programming problem and solved. The time and space complexities of our algorithm are \(O(n^2)\) and \(O(n + k)\) respectively, where \(n\) is the number of terminals in the routing region and \(k\) is the total number of cross points and via candidates.

References

Automatic Test Generation Using Neural Networks

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ABSTRACT

We describe a new automatic test pattern generation (ATPG) methodology that has the potential to exploit fine-grain parallel computing and relaxation techniques. Our approach is radically different from the conventional methods used to generate tests for circuits from their gate level descriptions. A digital circuit is represented as a bidirectional network of neurons. The circuit function is coded in the firing thresholds of neurons and the weights of interconnection links. This neural network is suitably reconfigured for solving the ATPG problem. A fault is injected into the neural network and an energy function is constructed with global minima at test vectors. Global minima are determined by a probabilistic relaxation technique augmented by a directed search. Preliminary results on combinational circuits confirm the feasibility of this technique.

REFERENCES
A Tool for Hierarchical Test Generation

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Abstract

An extended system and its algorithms for automatic test generation are presented. In a hierarchical mixed-level approach (from gate- to system-level) test patterns for sequential circuits of arbitrary depth, and even test programs for either external or self-test of microprocessor boards or processor systems can be generated automatically. In a complete hierarchy lower bounds for test coverage are easily computable. Numerous applications and first uses in real production line testing have shown good results.

References
**Test Generation for Sequential Circuits Using Individual Initial Value Propagation**

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**ABSTRACT**

This paper describes a test generation and fault simulation method which detects faults in the clock control logic that can cause register initialization failure in sequential circuits. By assigning an individual initial value Xn to the inaccessible register n in the faulty circuit and observing both the fault signal 0/Xn (0 in the good circuit / Xn in the faulty circuit) and 1/Xn in a different time frame, test vectors which can detect previously undetectable faults can be generated.

Consequently, this method can generate test vectors with 98% to 100% fault coverage for sequential circuits for which conventional test generation methods generate test vectors with 89% to 95% coverage.

**REFERENCES**

NCUBE: An Automatic Test Generation Program for Iterative Logic Arrays

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ABSTRACT

Iterative logic arrays (ILAs) are ideal as VLSI sub-systems because of their regular structure. Many functional modules such as multipliers are usually designed as ILAs. Deriving high quality tests for such large blocks of logic circuitry is very difficult. This paper presents an automatic test pattern generation program for general iterative logic arrays called NCUBE. NCUBE applies all possible input patterns to each array cell while ensuring that the effects of incorrect transitions are observable at the array outputs. If the array is testable with a constant number of test vectors irrespective of its size (C-testable) then NCUBE generates the constant size test set for the array. If the array cannot be tested with a constant number of test vectors then the test size is proportional to either the number of rows or the number of columns of the array or to the number of cells. In that case, NCUBE generates a minimal or near-minimal test set that depends on the size of the array.

REFERENCES

First Order Nonlinear Device Bypass in Circuit Simulation

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ABSTRACT

It is shown that the current bypass scheme used in SPICE produces inconsistent approximations to the function and derivative values needed by Newton iteration. A consistent first order bypass approach based on the first degree Taylor polynomial at the previous evaluation point is introduced. Test results show moderate reductions in the number of time points and Newton iterations during transient analyses, an increase in the percentage of devices that bypass, and a significant decrease in the average relative error of output waveforms. This last result suggests that comparable accuracy can be achieved with a considerably larger setting of the user-settable accuracy parameter, leading to a significant decrease in cpu time.

REFERENCES

A Dormant Subcircuit Model for Maximizing Iteration Latency

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ABSTRACT

We present a new approach for modeling dormant subcircuits, in circuit simulation, that utilizes iteration latency to provide speed improvements that are comparable to the potential speed improvements of an independent time step approach, without the associated disadvantages. This scheme minimizes the work required on the first iteration at a time point, the normal limiting factor in iteration latency schemes. However, since simulations are performed for each subcircuit at each time point, the penalty for backing up when truncation error is unacceptable, one of the nagging problems for independent time step approaches, is minimized.

References
Pyramid - A Hierarchical Waveform Relaxation-Based Circuit Simulation Program

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Abstract

A hierarchical waveform relaxation-based method for analysis of bipolar, MOS, and GaAs FET circuits is presented. By analyzing the circuit in a hierarchical manner, we have obtained faster solution of circuits exhibiting strong bidirectionality and feedback than had previously been possible. The technique has been applied to solution of a wide variety of digital and mixed analog/digital circuits. Using the hierarchical waveform relaxation method, we have been able to analyze circuits containing over 18,000 transistors. Results obtained for a variety of circuits show up to two orders of magnitude improvement in computation time compared to conventional circuit simulation techniques and up to one order of magnitude improvement compared to the standard waveform relaxation technique.

REFERENCES
An Envelope-Following Method for the Efficient Transient Simulation of Switching Power and Filter Circuits

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Abstract

The transient behavior of circuits like switching power converters and switched capacitor filters are expensive to simulate because these circuits are clocked at a frequency whose period is orders of magnitude smaller than the time interval of interest to the designer. It is possible to reduce the simulation time without compromising accuracy by exploiting the property that the behavior of such a circuits in a given high frequency clock cycle is similar, but not identical, to the behavior in the preceeding and following cycles. In particular, the "envelope" of the high-frequency clock can be followed by accurately computing the circuit behavior over occasional cycles. In this paper the implementation of such an envelope-following method that is particularly efficient for switching power and filter circuits is described, and results demonstrating the method's effectiveness are presented.

References

Floorplan Design Using Distributed Genetic Algorithms

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ABSTRACT

This paper presents a method to solve the floorplan design problem using distributed genetic algorithms. A series of experiments demonstrated that our method performed consistently better than a recently published simulated annealing approach, both in terms of the average cost of the solutions found and the best-found solution.

REFERENCES
Automatically Extracting Structure from a Logical Design

Mark Hirsch, Daniel Siewiorek
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Abstract

This paper presents an algorithm for extracting structure from a logical design. The algorithm uses a data structure which explicitly represents a variety of information generated during logical design in addition to connectivity. An example of the application of the algorithm to a UART design and its influence on layout is given.

References
Hierarchical Placement for Macrocells: A "Meet in the Middle" Approach

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ABSTRACT

This paper describes placement and related aspects of the BEAR macrocell layout system. A combination of top-down and bottom-up heuristics is used to make best use of a hierarchical description. The interdependency of placement and routing is considered explicitly. Experimental results show a considerable improvement over previous approaches.

References

Automatic Synthesis and Technology Mapping of Combinational Logic

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ABSTRACT

This paper describes SKOL, a system for the synthesis of combinational logic using a library of cells, with emphasis on the technology mapping algorithms. It combines current multilevel optimisation techniques with a new approach to the technology mapping problem. Each factor (of the factorised Boolean equation) can be implemented isolatedly or collapsed into the higher-level expression containing it, which is then implemented. An expression can be implemented in several ways, which differ in the degree of factorisation. A number of selected implementations is evaluated and the one with minimal cost (area or delay) is chosen. The mapping algorithms are independent of the library of cells, which can be easily modified. Results from benchmark examples were better than or comparable to existing systems.

REFERENCES

ABSTRACT

This paper presents a new approach to technology mapping, the process of making a standard-cells IC implementation from a previously optimized and decomposed set of Boolean functions. Instead of trying to solve the problem for random libraries of standard-cells, which proved to be very difficult, we have solved it for cell generators, which are only limited by technology constraints. The 'completeness' of the sets of cells, which can be generated by a cell generator given a certain technology, makes it possible to use an elegant algorithm.

The algorithms have been coded in CommonLISP, and used to map a large number of benchmark examples. The results are presented and they compare favourably with similar published results.

REFERENCES

Input Assignment Algorithm for Decoded-PLA's with Multi-input Decoders

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ABSTRACT

A decoded-PLA, i.e., a PLA which has decoders in front of an AND array, generally requires a smaller area than a standard PLA for realizing a function. However, it is usually very difficult to assign input variables to decoders such that the area of the decoded-PLA is minimal. An algorithm for assigning variables to decoders has been known to produce good results [10], but the number of inputs of the decoders was restricted to two and the area overhead of decoders, which is in fact quite significant, was not considered. This paper presents a heuristic algorithm for assigning input variables to the decoders of a decoded-PLA. In this algorithm, the number of inputs to each decoder is not restricted to two and the area overhead incurred by using multi-input decoders is considered in the cost function. Experimental results show that the areas of PLA's are smaller in many cases by using multi-input decoded-PLA's designed by this algorithm than those of decoded-PLA's with two-input decoders or standard PLA's.

REFERENCES
PLA Optimization Using Output Encoding

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Abstract

PLA's are widely used for automatic synthesis and layout of logic because of their conceptual and structural regularity. Earlier studies have focused on logic minimization of PLA descriptions and topological partitioning of the resulting layout. We have developed an automatic tool that heuristically determines a good partitioning of a single large PLA into a PLA with a smaller number of encoded outputs (and usually fewer product terms), followed by a set of decoders to regenerate the original outputs. Initial results using logic descriptions of processor chips developed at U.C. Berkeley and a benchmark set of industrial PLA's show area savings of up to 35% and delay reductions of up to 45%. The approach can be considered an alternative to Boolean decomposition and factoring in multi-level logic synthesis.

References
ECSTASY: A New Environment for IC Design Optimization

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Abstract

A new environment for IC design optimization is presented. Interfacing to SPICE3 with sensitivity computation capability, the system features (1) forms-based, menu-driven user interface for problem formulation and user interaction, (2) superlinearly convergent gradient-based algorithms and robust controlled random search procedure for circuit optimization.

References
A Symbolic Analysis Tool for Analog Circuit Design Automation

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Abstract

An analysis tool has been developed to generate symbolic design equations for analog circuits. This tool (SYNAP) works in conjunction with a symbolic mathematics program (MACSYMA) to create both exact and simplified analytic expressions needed for circuit design and forms the cornerstone of a non-fixed-topology analog circuit design system. SYNAP performs DC, AC, noise, and offset analyses for time-invariant analog circuits with one stable operating point and generates code for this new design system.

References
Analog Circuit Synthesis for Performance in OASYS

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ABSTRACT

This paper describes mechanisms needed to meet aggressive performance demands in a hierarchically-structured analog circuit synthesis tool. Experiences with adding a high-speed comparator design style to the OASYS synthesis tool are discussed. It is argued that design iteration—the process of making a heuristic design choice, following it through to possible failure, then diagnosing the failure and modifying the overall plan of attack for the synthesis—is essential to meet stringent performance demands. Examples of high-speed comparators automatically synthesized by OASYS are presented. Designs competitive in quality with manual expert designs, e.g., with response time of 6 ns and input drive of 1 mV, can be synthesized in under 5 seconds on a workstation.

References
ABSTRACT

With the emergence of consumer digital audio products, particularly compact disc and digital audio tape, comes the need for high resolution D/A and A/D converters. This paper presents a high-level synthesis tool, CLANS, that accepts data converter performance specifications and generates the optimal selection of block-level component specifications for the noise-shaping coders, the most popular A/D and D/A topology for digital audio. CLANS both predicts the performance of multi-bit noise-shaping coders (both A/D and D/A converters) and determines optimal loop filter transfer functions. The performance of CLANS' designs has been verified using both block-level simulation and experimental measurements on a CMOS prototype D/A converter.

References
An Improved Objective Function for Mincut Circuit Partitioning

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Abstract

We have developed an improved objective function for mincut circuit partitioning. We added the new objective function to the Kernighan-Lin, Fiduccia-Mattheyses (KLFM) partitioning algorithm. The time complexity of the enhanced KLFM algorithm remains linear in the number of pins and there is essentially no change in the CPU time requirements. Based on circuit bipartitioning tests with ten industrial circuits, the number of nets cut was reduced by as much as 55 percent when the KLFM algorithm used the new objective function. The average reduction in nets cut was 38 percent.

References

GORDIAN: A New Global Optimization / Rectangle Dissection Method for Cell Placement

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Abstract

A new placement method for cell-based layout styles is presented. It is composed of alternating and interacting global optimization and partitioning phases. In contrast to other methods using the divide-and-conquer paradigm, it maintains the simultaneous treatment of all cells during optimization over all levels of partitioning. In the global optimization phases, constrained quadratic optimization problems are solved having unique global minima. Their solutions induce the assignment of cells to regions during the partitioning phases. For general-cell circuits, a highly efficient exhaustive slicing procedure is applied to small subsets of cells. The designer may choose a configuration from a menu to meet his requirements on chip area, chip aspect ratio and wire length. Placements with high area utilization are obtained within low computation times. The method has been applied to general-cell and standard-cell circuits with up to 3000 cells and nets.

References


Simulated Annealing: a Fast Heuristic for Some Generic Layout Problems

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Abstract

There are two major criticisms about simulated annealing as a general method for solving combinatorial optimization problems: its effectiveness when compared with other well-designed heuristics and its excessive computation time. In this paper, we show that simulated annealing, with properly designed annealing schedule and move generation strategy, achieves significant speedups for high quality solutions when compared with tailored heuristics on two well-studied problems: the traveling salesman problem and the graph partition problem. Efficient heuristics for the traveling salesman problem can be applied to power and ground routing and, for the graph partition problem, to min-cut placement and logic partitioning.

References

Temperature Measurement of Simulated Annealing Placements

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Abstract

One way to reduce the computational requirements of Simulated Annealing placement algorithms is to use a faster heuristic to replace the early phase of Simulated Annealing. Such systems need to know a starting temperature for the annealing phase that makes the best use of the existing structure, yet does an appropriate amount of improvement. This paper presents a method for measuring the temperature of an existing placement based on analysis of the probability distribution of the change in cost function. Using this view a new definition of equilibrium is given and the equilibrium temperature of a placement is defined. Temperatures of placements produced both by a Simulated Annealing and a Min-Cut placement algorithm are measured.

References

A New Formulation of Yield Enhancement Problems for Reconfigurable Chips

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Abstract

An increase in chip density leads to an increase in the likelihood of introducing defective elements in a chip. Since, under most circumstances, only a small number of the elements in the chips are defective [Schu78], one way to enhance the yield of chip production is to use reconfigurable chips in which there are redundant elements that can be used to replace the defective elements. There are many different ways to reconfigure a chip using redundant elements. The covering problem is to assign redundant elements to replace the defective elements such that the chip will function properly. In this paper we introduce a general model that can be used to represent the relationship between redundant elements and defective elements in a uniform way. This model subsumes many of the models discussed in previous approaches. We give a complete characterization of the complexity of the covering problems in all the subcases of our model, most of which have not been studied before. It is hoped that the new formulation will also lead to new ways of designing reconfigurable chips.

REFERENCES:
Diagnosis and Repair of Memory with Coupling Faults

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Abstract

This paper addresses the problem of diagnosis and spare allocation for random access memory (RAM) with coupling faults. In the last two years a number of spare allocation algorithms for RAM with row and column redundancy have been proposed. These procedures, however, have been restricted to repairing stuck-at faults. This paper is unique in that it examines both diagnosis and repair of coupling faults in RAMs utilizing spare rows and columns. In this paper we show that a coupling fault is repaired if its coupling cell is replaced by utilizing a spare row or its coupled cell is replaced by utilizing a spare row or column. By specifying both the coupled cell and coupling cell the amount of redundancy required to repair a given set of faults may be reduced. A diagnosis procedure for RAM is provided to locate stuck-at faults as well as coupling faults. A graph model is employed to describe the repair of coupling faults and a repair procedure has been implemented to allocate rows and columns for repair.

References

Two-Layer Quad Trees: A Data Structure for High-Speed Interactive Layout Tools

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ABSTRACT

This paper describes a Two-Layer Quad Tree data structure which creates an effective search environment for both region queries and size queries. A corner-based sorting method resolves the Quad Tree bisector list problem. A region growing technique reduces region query search overhead. A two-layer Quad Tree implementation improves size query speed. Experimental results show that these techniques significantly improve query speed for both classes of queries.

REFERENCES
The Use of Inverse Layout Trees for Hierarchical Design Verification.

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Abstract

This paper presents the inverse layout tree as a means of performing fully hierarchical design verification without any restrictions on subcell overlaps. This provides us with a fast and general method of marking design rule errors or extracted devices at the correct hierarchical level. The inverse layout tree for each element is built up as layout data is processed from the bottom up. When layout processing is completed we can go through the layout again and use the inverse layout trees to determine the most appropriate cell for each element. New elements formed as layout from different cells overlaps can now be placed at the lowest level of hierarchy where they always appear instead of being indiscriminately incorporated in the parent cell. Thereby, the method using inverse layout trees preserves the original hierarchy to the largest possible extent. The method has been implemented in our corner-based design-rule checker (DRC) and circuit extractor, Corny. As an important example we show that logical DIFF (ANDNOT) operations between layers can be performed fully hierarchically.

References
Expanded Rectangles: A New VLSI Data Structure

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J. Solworth
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ABSTRACT

This paper presents a new data structure derived from corner stitching which enables efficient representation of VLSI layouts. While each entry in the expanded rectangle data base is larger than the corresponding corner stitched entry, generally fewer entries are required to represent the same VLSI layout. The data structure has two important features: first, the VLSI design is represented as a slicing structure in which each slice contains a portion of the solid material; and second, corner stitches are used to provide two dimensional nearness information. Initial measurements indicate that expanded rectangles is a viable data structure for use in a complete VLSI layout system.

REFERENCES
Automatic Layout of Custom Analog Cells in ANAGRAM

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ABSTRACT

ANAGRAM, a tool for full-custom layout of analog cells, is described. ANAGRAM models cell layout in the style of a macro-cell place and route problem. Individual cell primitives (transistor-level objects of widely varying sizes) are the macro-cells. Module generation techniques are employed to generate these internal primitives, and to preserve critical matchings and symmetries. An annealing-based placement algorithm then places these primitives, and is followed by a novel line-expansion signal router. The router includes mechanisms to avoid noise coupling due to internodal capacitances between the signal wires and shared parasitic resistances in the DC supply wiring, and operates in an iterative improvement fashion to eliminate such violations. Layouts for several custom CMOS cells have been successfully generated. Circuit simulation results based on cell extractions demonstrate the effectiveness of the crosstalk avoidance mechanisms.

References
Automatic Layout Generation for CMOS Operational Amplifiers

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Department of Electrical Engineering and Computer Sciences, University of California, Berkeley

ABSTRACT

An analog silicon compiler for CMOS op amps (OPASYN) has been developed. The synthesis system takes as inputs system-level specifications, fabrication-dependent technology parameters, and geometric layout rules. Based on the general domain of the specifications, the program first selects an appropriate circuit topology from a database and determines optimal values for the set of design parameters so as to meet the design objectives. Subsequently, a mask-level layout for the given circuit with its optimized device sizes is constructed using an approach based on a few leaf cell generators and on circuit-dependent slicing trees that guarantee sound arrangements of the individual generated components. The synthesis process is fast enough for the program to be used interactively at the system design level by system engineers who are inexperienced in op amp design.

REFERENCES