Programmable Frequency Divider for PLL Applications
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Abstract—Today, the trend is developing whole Systems on a Chip (SoC), that is: integrate all the electronic system’s functions, including digital and analog circuits, on a single silicon die. The Application Specific Integrated Chip (ASIC) is the back end process of the VLSI technology. The ASIC design aims at the designing the customized digital and analog IC for application specific. This paper proposes the design & implementation of a programmable frequency divider (PFD) for PLL applications operating at 100MHz. Here the prescaler architecture is designed & this architecture is applied to a 5/6 dual modulus prescaler to obtain a particular range of clock frequencies. This PFD has been implemented using 0.18um TSMC CMOS technology with the power consumption of about 0.96mW under 3.3V power supply. Measurement results show that it is very successful in planned frequency division.

Index terms— Programmable frequency divider (PFD), prescaler, Pulse-Swallow Architecture.

I. INTRODUCTION

Phase-Locked Loops (PLLs) are functional circuit that generates signals phase-locked with external input signals. They are widely used for synchronization purposes and are essential in communication field. Owing to the broad use of mobile electronic systems, low-power consumption and low jitter have become the main concern in PLLs design. Besides, fast lock time is required in nearly all PLL applications. PLLs are generally built of a phase frequency detector, a charge pump, a low pass filter, a level shifter, a voltage-controlled oscillator, and a frequency divider in the feedback path.

The dual modulus prescaler system is used as the divider in a phase locked loop (PLL) [1]. The main reason for its use is to allow a higher reference frequency for the loop. The higher reference frequency gives better frequency stability by supplying more samples per unit time to the phase detector. Due to the high operation frequency of the frequency dividers, they usually consume much more power than the other components in PLLs.

In this paper, a programmable frequency divider (PFD) is implemented for PLL application, based on standard cells and then integrated with other modules which are designed with full custom method to construct an integer frequency divider. Measurement and simulation results indicate that this PFD works well in the frequency synthesizer [7]. With that, the frequency synthesizer can perform multimodulus division and can be employed in multistandard applications. The digital frequency divider is usually realized by cascading divide-by-2 circuits for high speed applications. However, this structure can only obtain the division ratios equal to n power of 2, where n is the number of divide-by-2 stages.

In order to obtain different division ratios, a dual-modulus prescaler (DMP) and a PFD are integrated in our design to realize a PLL frequency synthesizer. In addition, an integer-N frequency synthesizer structure is adopted in this design. It is because the integer-N frequency synthesizer is more practical with less cost and lower spurious sideband effect compared to fractional-N frequency synthesizer. In this way, the dividers can obtain any division ratio based on the outside control signal.

RF design has traditionally been done in Bipolar or Gallium Arsenide (GaAs) technologies and SiGe-Bipolar process is also gaining widespread acceptance. Complementary-Metal-Oxide-Semiconductor technology is a cheaper alternative to other commercially available IC fabrication processes.

There is a growing financial incentive to develop single-chip transceivers, high-speed microprocessors, fiber optic sub-systems and complex Systems-On-Chip (SoC) using CMOS technology. CMOS is an area of active research driven primarily by the wireless market. CMOS is the technology of choice for consumer electronics, microprocessors, networking, memories and video clock generators because of its very low power dissipation and cost.

II. PROGRAMMABLE FREQUENCY DIVIDER (PFD)

A frequency divider is an electronic circuit that takes an input signal with a frequency, \( f_{in} \), and generates an output signal with a frequency:

\[
    f_{out} = \frac{f_{in}}{n}
\]

where \( n \) is an integer. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog and digital applications.

A frequency divider is employed in the Phase-Locked Loop to reduce the reference frequency and provide necessary programmability of the synthesizer, both in an integer-N or a fractional-N structure [2]. It is worth noticing that a frequency divider is one of the two only blocks in a frequency synthesizer that need to run at full speed. The other is the voltage controlled oscillator (VCO).

Because the divider runs at the same frequency as the VCO, the design of this circuit is difficult and often determines the maximum usable frequency of the PLL synthesizer. The choice of the divider architecture is essential for achieving low-power dissipation, high design flexibility of existing building blocks. Usually, the first or
first few stages of the divider are fixed frequency divider, called prescaler. The rest of the divider is programmable and often based on a variant of dual modulus division techniques.

A divider can be achieved by using a programmable counter. A complete divider consisting of a fixed divider cascaded with a programmable divider.

Resolution (Complete divider) = Resolution (programmable divider) x Division ratio (fixed divider).

Here Dual modulus prescaler is used. A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal (modulus control signal). By using the dual-modulus prescaler with an Swallow 'S'(N1) and Programmable 'P'(N2) counter one can still maintain good resolution and programmability becomes easier (for division factor fewer bits needed to programmed).

A. Dual-Modulus Operation:
A programmable dual modulus divider includes an N/N+1 prescaler & two programmable down counters. (S & P counters) as shown in the Fig. below.

The divider works as follows. As long as the S counter has not timed out, the prescaler divides down by N+1. So, both the S and P counters will count down by 1 every time the prescaler counts (N+1) VCO cycles. This means the S counter will time out after ((N+1) S) VCO cycles. At this point the prescaler is switched to divide-by-N mode. The P counter still has (P - S) cycles to go before it times out. So after ((P - S) N) more cycles, the system is now reset to the initial condition. Expressing the above discussion mathematically, total number of VCO cycles for one dual-modulus division, is

\[ M = (S + PN) \]  

\[ = (SN + S + PN - SN) \]  

B. Pulse-Swallow Architecture
One important factor that has not been addressed yet is how the dual-modulus operation can be implemented. The conventional implementation of any divider/prescaler is using digital counters. The division factor that can be easily realized using such logic is of the form 2^N, i.e. the pattern in which the counter counts repeats every 2^N cycles. To implement 2^N + 1, therefore, one extra state of the system needs to be inserted over single pulse duration in the repetitive pattern. This is referred to as a “pulse-swallow” operation.

The principle of operation of the pulse-swallow architecture can be explained by means of a simple divide-by-2/3 circuit. Fig. 3 shows the simplest divider, an ÷2 implemented with a D flip-flop.
III. ACTUAL IMPLEMENTATION

A programmable dual modulus divider includes an N/N+1 prescaler and two programmable down counters (N1counter, N2counter). Here, 5/6 frequency divider, a 5-bit and a 3-bit counter is been used to form the frequency divider.

A. The High Level Design

The Programmable frequency Divider which is designed here uses Dual modulus Prescaler, Swallow counter and Programmable counter.

A reference frequency of 1MHz is used for the frequency synthesizer and for VCO output frequency range 50-100MHz, so the Divider should provide division should between 50-100. The divider is designed using Prescaler, Swallow counter and Programmable counter. The divider ratio of the programmable frequency divider is given by M=PN+S, where P is Programmable counter count value, S is Swallow counter count value and N represents N/N+1 prescaler.

By using 5/6 prescaler, programmable bits can be reduced compared to 2/3 prescaler. For division ratio M=50-100, using 5/6 prescaler, P can be chosen between 10-20, and S can varied between 0-5. By fixing P at a particular value between 10-20, just by varying S between 0-5 (programming 3bits) we can get 5 different division values easily. So the divider is designed using 5/6 prescaler, 5 bit programmable counter and 3 bit swallow counter. The programmable and swallow counters used here are loadable down counter.

B. Input/output explanation

Input “P1 ~ P5” set the count number of 5-bit counter & input “S1 ~ S3” set the count number of 3-bit counter which can be varied from 0-7. Here, P is set to 24, i.e. (11000)2

Input “Fin” feeds input signal (whose frequency is to be divided.)

Input “load” resets loaded number of counter when switching divide ratio.

Output “Fout” is the input signal after divided, i.e., the output of the divider.

C. Block explanation

The swallow counter is a programmable counter and is used in order to obtain a variable and externally controlled division rate. The input signal is the output of the prescaler and is generally controlled by an external input and by a reset coming from the program counter.

Block “div5_6” operates in the highest speed. It divides the input signal frequency by 5 when “mode” = 0 and divides the input signal frequency by 6 when “mode” = 1.

Block “programmable counter” is triggered by output of div5_6. When programmable counter (P counter) counts to ‘0’, the load signal goes from low to high to reload P counter and swallow (S) counter, i.e. initially all outputs of P-counter is zero, so the output of 5input NOR is 1, hence it will load the inputs in S-Counter and P-counter.

When the output of 5input NOR gate output becomes “0”, count pin in S-counter and P-Counter will be set to “1”. Hence the count operation starts.Function of 5input NOR gate ends.

Block “S counter” is triggered by output of or (NOR & NOT). When S counter counts to ‘0’, the “mod” signal goes from high to low to change divide ratio of div5_6 from 6 to 5.

Until P counter counts to ‘0’, the counter is reloaded, the “mode” signal will return to high. And the divide ratio of div5_6 returns to 6. (depending on the S1,S2 and S3 inputs of S-counter, mode is adjusted, which in turn divides the input frequency either by 5 or 6. i.e., divides by 5 if Mode=0 and divides by6 Mode=1)

Function of 5/6 prescaler: Works as Frequency Divider, constructed using two 2/3 prescaler, also called as Multi-Modulus Divider because of Mode select signal to select Division ratio.

Output of 5/6 prescaler is used as a Clock input to P-Counter, here in P-Counter it will divide clock further according to M (i.e. M=55)

A division ratio i.e. M=55 appears on O2,line. The final output frequency hence obtained is 1.82MHz.

D. Design circuit description (Low Level Design)

This section provides the design & implementation of 2/3 & 5/6 prescaler.

Div5_6:
The 5/6 designed using 2/3 prescaler. An n-bit MMD (Multi-Modulus Divider) is a modular structure consisting of a chain of 2/3 divider cells connected like a ripple counter as shown in Fig. 7.

![Fig. 6. PFD Top block diagram.](image)

The multi-modulus divider operates as follows. In every division period, the last cell of dual modulus prescaler in the chain generates signal modn−1. This signal then
propagates up the chain. An active mod signal would enable the cell to divide by three once in a division cycle, as long as the programmable input bit \( p \) is set to 1. In other word, the dual-modulus divide-by-2/3 cell would divide by three only ONCE in a whole division cycle, if it ever gets enabled to do so by having both the programmability \( p \) and the signal mod enabled. For the rest of the division cycle, the cell divides the input by two. Thus, division-by-three action only adds one extra period of each cell’s input signal to the period of output signal. For example, each divide-by-three action in a cell with a 2.5 GHz (0.4ns period) input would introduce an extra 0.4 ns to the output period. The output period then becomes 1.2ns instead of 0.8 ns.

Applying the principle to the whole chain, the output period can be calculated as in equation as shown below.

\[
T_{\text{out}} = 2^n \cdot T_{\text{in}} + 2^n - 1 \cdot T_{\text{in}} \cdot p_{n-1} + 2^n - 2 \cdot T_{\text{in}} \cdot p_{n-2} + \cdots + 2 \cdot T_{\text{in}} \cdot p_1 + T_{\text{in}} \cdot p_0
\]

In the above equation, \( T_{\text{in}} \) is the period of the input signal, \( p_0, \cdots, p_{n-1} \) are the binary programming bits for cell 1 to n respectively. The equation shows that all integer division ratio ranging from \( 2^n \) to \( 2^n + 1 - 1 \) can be realized. For example, for the former to happen, all \( p_n \) should be set to zero, while that latter could be achieved by setting all \( p_n \)’s to one. The modular architecture of figure 3.1 can be applied in the realization of programmable frequency dividers for fractional-N synthesizers. Here, the division ratio required is 55. Hence we go for 5/6 prescaler which is constructed using 2/3 prescaler.

Let’s first look into 2/3 divider. Based upon the fundamental structure mentioned above, a dual-modulus divide by- 2/3 prescaler cell (modular approach) could be realized with as in figure below.

![Fig. 8. Prescaler Logic.](image)

The dual-modulus prescaler consists of two functional blocks, the prescaler logic and the end-of-cycle logic. The prescaler logic block divides, upon control by the end-of-cycle logic, the frequency of the input clock by either two or three, and sends the divided output signal to the next cell in the chain. The end-of-cycle logic decides the instantaneous division ratio. The mod\(_{in}\) signal is active once in a division cycle. The enable signal of programmability \( p \) is checked at the moment mod\(_{in}\) is active. Based on its status, the end-of-cycle would send or not send a feedback signal to prescaler logic cell to force it swallow one extra input clock period. It is also worth noticing that regardless of the state of \( p \) input, the prescaler would re-clock the mod\(_{in}\) signal and send and output mod\(_{out}\) signal to its proceeding cell in the chain. Now, we have a 2/3 divider, by using which, a 5/6 prescaler is constructed which is as shown in the Fig. 9.

![Fig. 9. 5/6 Prescaler.](image)

Depending on the mode signal, the input frequency (i.e. \( F_{\text{in}} \)) gets divided either by a factor of 5 or 6. For ex: say mode=0 due to which, the output of the inverter goes high.

Due to which inputs to the OR gate are 0 & 1 which drives the output of OR gate to 1. Hence one of the 2/3 prescaler will be active & another 2/3 acts as stand alone (reset), since there is a NOT gate connected in b/w the output of the OR gate & the 2\textsuperscript{nd} 2/3 prescaler.

Hence, depending on the mode select & the Fo (i.e. fout) signal coming from the 2/3 prescaler, the input frequency gets divided, i.e., it acts as divide by 5 when mode=0 & divide by 6 when mode=1

IV. EXPERIMENTAL RESULTS AND ANALYSIS

In this section, simulation results of programmable frequency divider is been discussed. i.e.

1. Simulation result of a programmable frequency divider.
2. Next, the simulation results of each block of the PFD, to analyze the working of each block.

A. Simulation result of a PFD

Figure 10 below shows the simulation result of a PFD which is observed on O\(_4\) line. Here, the input frequency is 100MHz. Since the division ratio is set to be 55, the output frequency is found to be 1.82MHz. Similarly, the simulation results observed on O\(_1\), O\(_2\), O\(_3\), O\(_5\) line are shown in the figure 11
Simulation results observed on o1, o2, o3, o5 output lines of P-counter.

B. Simulation – reset divide ratio

In this section, it’s been observed to check if the frequency divider can change divide ratio in a short time at any timing. Here, the input frequency is 100MHz. It’s been observed that the frequency divider will change divide ratio and work correctly each time we raise reset signal.

C. Simulation result of 5/6 Prescaler

At typical corner case,

The input frequency is 100MHz & Vdd=3.3V.
S=7, P=24 & N=2.
Since the divider ratio, M=S+PN, we get M= 7+24*2=55, hence, fout=1.82MHz.
Power dissipation of the Divider = 0.96mW

V. CONCLUSION

In this paper, the design of a low-cost, high speed programmable frequency divider has been presented. It is implemented in TSMC 0.18μm CMOS technology. Simulation results have been presented for the frequency divider. Simulation results indicate that the frequency divider achieves the expected precision. Primarily this frequency divider is used for PLL applications & works well when this PFD is mixed with other modules designed with full custom method.

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