An On-Chip Delay Measurement Technique Using Signature Registers for Small-Delay Defect Detection

Kentaroh Katoh, Member, IEEE, Kazuteru Namba, Member, IEEE, and Hideo Ito, Member, IEEE

Abstract—This paper presents a delay measurement technique using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18-μm process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design on average. The area overhead is 23.4% larger than that of the delay measurement technique using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.

Index Terms—Delay estimation, design for testability (DFT), integrated circuit measurements, semiconductor device reliability, signature register.

I. INTRODUCTION

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems [1]. If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, enhancing the quality of the testing for the small-delay defect detection is an urgent need.

The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects [2]. However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore, development of the embedded delay measurement technique is required.

Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques [3]. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical. Noguchi et al. proposed the self testing scan-FF. The flip flop reduces the required number of scan operations, which makes the measurement time practical [2]. They also proposed the area reduction technique of the self testing scan-FF [4]. However, the area overhead of these methods is still expensive compared with the conventional scan designs.

This paper presents a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

The rest of this paper is organized as follows. In Section II, preliminaries are discussed. Section III explains the proposed method. Section IV shows the experimental results. Finally, Section V concludes this paper.

II. PRELIMINARIES

A. Related Works

These days, various methods for small-delay defect detection have been proposed. The path delay fault testing with a normal clock width is the most popular and is widely used [5]. In this
method, we choose the longer paths to detect the smaller cumulative delay due to the small delay distributed on the paths. The larger the cumulative delays, the higher the probability of the detection of the distributed small delay. However, the coverage of the small delay defect detection largely depends on the normal clock width, which is a problem of this method.

On the other hand, to solve the problem, methods with delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore the smaller delay defects which cannot be captured with the normal clock width can be captured with the appropriate smaller test clock width.

Liou et al. proposed a small-delay defect detection method consisting of two test phases using both a tighter test clock and a normal clock [6]. In this method, the transition delay fault testing with a tighter test clock width which is calculated based on the characterized delay distribution is applied in the first phase. After that, path or transition delay fault testing is applied with a normal clock width in the second phase. The quality of the method is higher than the conventional one phase test with normal clock width. Yan et al. proposed a delay testing scheme that identifies small-delay defects in the slack interval by comparing switching delays of a neighboring die on a wafer [7]. In this method, a fault site is sensitized multiple times continuously with reducing the test clock width by the slack interval. The abnormal switching delays are detected by comparison with the test results in the neighboring die. Another work detects small-delay defects by analyzing the failing frequency, which is the minimum frequency that the delay fault testing fails when the path is sensitized multiple times continuously with increasing the test clock frequency [8]. Generally, the variable clock testing requires a variable on-chip clock generator. Various variable on-chip clock generators have been proposed [9]–[12]. In variable clock testing, the test clock frequency should be optimized to each test vector. To improve the test quality, various optimization methods of the test clock and test set have been proposed [13]–[15].

These days, small-delay defect detection methods using on-chip delay measurement techniques have been proposed. The direct measurement of the real delay of each path of each chip screens outlier chips robustly even in the presence of process variation or the gap between real and simulation environment. It realizes higher fault coverage of small-delay defects than the simulation-based ones.

In addition, it can be used not only for the detection of small-delay defects, but also for the debugging [16], [17]. Because modern chips are too huge and complex, LSI CAD tools can not optimize the design enough. Hence, the manufactured first silicon chip usually does not meet the specification in spite of the tighter release to production (RTP) schedule. Therefore silicon debugging and design for debugging (DFD) become much more important in modern chips [18]. Various silicon debugging technologies and DFD methods have been proposed [19]–[22]. On-chip delay measurement provides accurate information of the delay of inside paths for the debugging of small-delay defects [23].

Most of the conventional works of on-chip delay measurement are classified to either a proposal of an embedded delay measurement circuit or that of a scan architecture for scan-based on-chip delay measurement with a variable clock generator.

Some works proposed embedded delay measurement circuits of modified vernier delay line (VDL). Datta et al. proposed the embedded delay measurement circuit with high resolution [24]. It is the first work of an embedded measurement circuit of modified VDL to the best of our knowledge. Tsai et al. proposed the area efficient and noise-insensitive modified VDL with coarse and fine parts namely BIDM [25]. Pei et al. also proposed the area efficient modified VDL. The feature of this method is delay range of each stage of VDL [26]. The delay ranges increase by a factor of two gradually, which reduces the required stages. Therefore the area is smaller than Datta’s work. The modified VDLs achieve high resolution. However they require redundant lines to feed the input and output signals of the measured paths, which needs the compensation of the delay effect of the redundant lines. Tanabe et al. solved the problem by removing the delay of the redundant lines from the measured delay using some additional embedded circuits [27]. The proposed technique is categorized to the scan-based one.

B. Variable Clock Generator

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method. In this paper, we use the on-chip variable clock generator proposed by Noguchi et al. [2].

Fig. 1 illustrates the circuit. The circuit consists of the phase-interpolator-based clock generator and the 2-pulse generator. The phase-interpolator-based clock generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal. Some of the specification and the evaluation results are shown in Table I [11].

C. Small-Delay Defect Detection With Delay Measurement of Chips

The proposed method uses the Noguchi’s small-delay defect detection technique [2]. In this technique, the test clock width...
TABLE I
SPECIFICATION AND MEASUREMENT RESULT [11]  

<table>
<thead>
<tr>
<th>Process</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Occupied area</td>
<td>300 [μm] × 128 [μm]</td>
</tr>
<tr>
<td>Input clock</td>
<td>1.5GHz 4phase</td>
</tr>
<tr>
<td>Output clock</td>
<td>1GHz to 2GHz 4phase</td>
</tr>
</tbody>
</table>

| Functions       | - Frequency control  
|                 | - Jitter generation  
|                 | - Duty ratio control  
|                 | - Phase control |

| Step error (5 chip measured) | ±1.3ps ~ ±2.4ps (±0.7° ~ ±1.3°) |
| Cumulative timing error (5 chip measured) | Best chip ±5.4ps ~ ±11.2ps  
|                                      | Worst chip ±2.9° ~ ±6.3° |

Fig. 2. Decision of test clock width based on path delay distribution obtained by chip measurement [2].

for delay fault testing of each path is determined with the normal path-delay distribution of each path.

This strategy has already been applied to various small-delay detection techniques [13].

But its originality is to obtain the path-delay distribution with the delay measurement of the paths of the fabricated chips. Fig. 2 shows the path delay distribution of a path obtained by the delay measurement of the fabricated sample chips. The horizontal axis is measured delay. The vertical axis is the number of chips. The chips which have delay inside the range Variation, namely Outliers0, Outliers1, Outliers2, are abnormal chips. The delay Outliers2 is the outside of the clock cycle in normal operation. Therefore it will be detected by conventional delay fault testing with the clock cycle in normal clock operation which is Conventional criteria. The delay Outliers0 and Outliers1 are within the clock cycle in normal operation. The conventional delay fault testing regards them as good chips. However because the delay is outside Variation, it will cause improper operations under particular operation in certain applications and may cause improper operations after shipping due to the effect of aging [2]. In Noguchi’s technique, the test clock cycle is set to the upper limit of the distribution of normal chips, which is New criteria. Then all the outlier chips are detected by the delay fault testing.

In small technology, the path-delay distribution calculated by simulation is different from that of the fabricated chips. Therefore the quality of its strategy is higher than that of simulation based ones. Because the Noguchi’s technique requires the measurement of the explicit paths, the paths should be single-path sensitzable [5]. The aim of the technique is to screen the chips which have abnormal delay in gates or wires. Therefore the test set for the measurement should detect all the transition faults which are sensitized through single-path sensitzable paths. The proposed method is a new delay measurement technique for the small-delay defect detection technique.

III. DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTERS

This section explains the proposed measurement method. Section III-A presents the concepts of the proposed method. Section III-B explains the implementation of the proposed method. Section III-C describes the measurement sequence. The data volume and area overhead should be realistic compared with the conventional scan designs for DFT. Section III-D explains the reduction method of the tester channel. Section III-E describes the scheme for the decision of the number of the required extra latches to keep the cost realistic. To apply the proposed method and realize short measurement time, some constraints should be put on ATPG. Section III-F explains the ATPG constraints. Section III-G describes the measurement time and data volume. Finally, Section III-H describes the test response tracing mode for finding lowest failing frequency or diagnosis with transition fault test vectors.

A. Basics

This section explains the concept of the proposed delay measurement. The target paths of the proposed method are single-path sensitzable [5].

Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement.

Fig. 3(a) shows the basics of the proposed method.

This example has three flip flops FF0, FF1, and FF2. Each flip flop has the input line, the output line, and the clock line clk. Each flip flop FF0 is connected to an extra latch. At first, we assume that each flip flop has its own extra latch. The value of each flip flop is stored in the correspondent latch, and the value of each latch can be loaded to the correspondent flip flops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be
loaded from these latches in a clock without scan-in operation. It reduces the time for multiple sensitization of a path drastically. The horizontal line through these flip flops represents the scan path. The symbols \(s_{ci}\) and \(s_{co}\) represent the scan input and output, respectively.

The rectangle SIG represents the signature register using the linear feedback shift register as its basic component. The input of SIG is connected to the output of the last flip flop FF2. More detail structures of the flip flops and the signature register are shown in Figs. 4 and 5, respectively.

Here, we measure the delay of \(p_1\). In this example, we assume that the clock width of normal operation is 10 ns, and the resolution of the delay measurement is 2 ns. First, SIG is initialized with reset operation. Second, the target path \(p_1\) is tested continuously 5 times with the test clock reduced gradually by the resolution. The multiple clock width testing is realized by the variable clock generator explained in Section II-B. The test clock of the 1st testing \((#1)\) is 10 ns. After the test, the test response is sent to SIG through the scan path with two clock shift out operation. The test clock of the second testing \((#2)\) is 8 ns. Similarly, the test clock width of the third, fourth, and fifth testings \((#3, #4, #5)\) are the difference between 2 ns and the previous test clock width. Each test response is sent to SIG with two clocks. After the above 5 times of delay fault testings, the signature value of SIG is retrieved. To estimate the delay, the retrieved signature value is compared with the expected signature values of the signature table. Fig. 3(b) shows the signature table in this example. The table has four columns. The first column is the cases of the measurement. The second column is the sequences of the test responses of the 5 times measurement shown in Table III. The symbols \(Cae_{01}, Cae_{02}, Cae_{03}, Cae_{04}, Cae_{05}\) indicate the cases with path delays, more than 10, 8–10, 6–8, 4–6, 2–4, 0–2 ns, respectively. The symbols \(P\) and \(F\) represent the pass and fail of a testing, respectively. In case of rising transition testing, \(P = 1\) and \(F = 0\), and in case of falling transition testing, \(P = 0\) and \(F = 1\). The retrieved signature value is compared with the expected signature values on the table, and decides the delay value.

When the number of flip flops is \(n\), clock width is \(T\), the measurement resolution is \(\Delta T\), and the continuous testing time is \(N_{\text{mns}}\), the delay measurement sequence of a target path is as follows. Here, we assume that the test vector is already stored in the latches. The end point of the measured path is \(\text{FF}_k(0 \leq k \leq n - 1)\).

- **Step 1**: Initializing SIG.
- **Step 2**: Test vector is loaded from the latches.
- **Step 3**: Test clock width \(T\) is set to normal clock width.
- **Step 4**: Test clock is applied.
- **Step 5**: The test response is sent to SIG which is connected to the output of \(\text{FF}_{n-1}\) with \(n - k\) clocks.
- **Step 6**: If testing time is equal to \(N_{\text{mns}}\), go to Step 7 after the signature value of SIG is retrieved, otherwise go back to Step 2 after the test clock width \(T\) is updated to \(T - \Delta T\).
- **Step 7**: The delay value is estimated by comparing the retrieved signature value and the signature table.

### B. Implementation

In this subsection, we explain the implementation of the proposed measurement system. First we explain the important components to understand the whole system. After that, the whole system is presented.

1) Scan Flip Flop for Measurement: Fig. 4 is the gate level description of the scan flip flop for the proposed measurement. The lines \(D, Q,\) and \(\text{clk}\) are the input, output, and clock lines, respectively. The line \(\text{latch}\) is connected to an extra latch which provides the test bit to the flip flop. The lines \(s_{i}\) and \(s_{o}\) are the input and output for constructing the scan path. The input \(s_{i}\) is connected to \(s_{o}\) of an adjacent scan flip flop or the scan input. The output \(s_{o}\) is connected to \(s_{i}\) of an adjacent scan flip flop or the scan output. The flip flop has two multiplexers. The lines \(s_{i}\) and \(\text{latch}\) are the inputs of the upper multiplexer controlled by \(s_{co}\). The output of the upper multiplexer and \(D\) are the inputs of the bottom multiplexer controlled by \(s_{co}\). When \(s_{co} = 0\), the flip flop is in normal operation mode. When \(s_{co} = 1\) and \(s_{co} = 1\), the flip flop is in scan operation mode. When \(s_{co} = 1, s_{co} = 0\), the flip flop loads the value stored in the latch connected to the latch line.

2) Reconfigurable Signature Register: The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.
- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

Fig. 5 shows the architecture of the signature register for the proposed measurement. The length of the signature register in this example is four bit. Therefore it has four flip flops \(\text{FF}_0, \text{FF}_1, \text{FF}_2, \text{FF}_3\).

The signature register can be configured to a shift register. The line \(sge\) controls the configuration. When \(sge = 1\), it works as a signature register. When \(sge = 0\), it works as a shift register.
The line \( in \) is the input of the signature register. During measurement, test responses are sent to \( in \). The line \( clk \) is clock line. The clock line is controlled by \( sclk \). When \( sclk = 0 \), the signature register does not capture the input value. When \( sclk = 1 \), the signature register captures the input value synchronizing with the positive edge of \( clk \). By controlling \( sclk \), the signature registers capture only the target test response.

When \( sgo = 0 \), this circuit is configure to the shift register. The input is \( sgo \). The output is \( sgo \). As explained later, the measurement system requires multiple signature registers generally. The input and output are connected to the output and the input of adjacent signature registers to construct a long shift register for sending all the signature values to the external tester.

3) Whole System: Fig. 6 shows the proposed measurement system. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) explained in Section II-B and a BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip flops and the signature registers independently. The reset operations are controlled by the tester.

The low cost tester controls the whole measurement sequence. The clock frequency \( tck \) is slower than the functional clock. The line \( sgo \) retrieves the signature data from the signature registers to estimate the measured delay. The line \( sc1 \) sends the test vectors to the scan input of the chip. The line \( sc0 \) gets the data of the flip flops from the scan output of the chip. In the proposed measurement sequence, \( sc0 \) is not used. However, it is used to check the flip flops or the additional latches before the measurement. The line \( cs \) is the clock control line. The proposed measurement uses both the slow tester clock \( tck \) and the fast double pulse generated by on-chip VCG. The line \( cs \) selects the slow and fast clock. If \( cs = 1 \), the fast clock is sent to the clock line \( clk \) of the components. Otherwise the slow tester clock \( tck \) is sent. The lines \( trg \) and \( cmi \) are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of \( trg \). The line \( cmi \) controls the width of the double pulse. The line \( sce \) controls the scan flip flops. The line \( lck \) controls the latches for storing test vectors. The lines \( sc0[0]\ldots sc0[n-1] \) are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers \( sc0[0]\ldots sc0[n-1] \). As explained later, the decoder is used to reduce the input lines for the control data of the signature registers. The \( sgo \) is the enable signal for the signature registers. The flip flops in the chip are classified to the clusters \( Cl_0\ldots Cl_{(m-1)} \). Here, we assume that each cluster has \( n \) flip flops, and thus the number of the flip flops is \( mn \). In general, the number of the flip flops of the last cluster is \( N_{FF}\ldots N_{m} \), where \( N_{FF} \) is the number of flip flops, or \( n \). The coordinate \((i,j)\) written in the flip flops indicates the location. The number \( i \) is the cluster id. The number \( j \) is the order in the cluster. The output of the flip flop of \((i,n-1)\) which is the tail flip flop of each cluster \( Cl_i \) is connected to the flip flop of \((i+1,0)\) which is the head flip flop of \( Cl_{i+1} \). These lines construct the scan chain. The output of the tail flip flop of each cluster is connected to the input of the corresponding signature register. The paths whose test response is captured by the flip flops included in \( Cl_i \) is measured by \( SIG_i \). The control lines of the signature registers are connected to the BCD decoder.

C. Measurement Sequence

Here, we explain the measurement sequence. First, the measurement sequence of the paths simultaneously sensitized in a test vector is explained in Section III-C1. After that, the whole measurement sequence is explained in Section III-C2.

1) Measurement Sequence Per a Test Vector: When the measurement system has \( m \) signature registers, \( SIG_0\ldots SIG_{(m-1)} \), \( m \) paths can be measured in parallel maximally. To reduce the measurement time, we measure multiple paths simultaneously.

We explain the measurement strategy using the example depicted in Fig. 7. In this example, the proposed method is applied to the circuit with six flip flops \( FF_0 \ldots FF_5 \). These flip flops are classified to the two clusters \( Cl_0 \) and \( Cl_1 \). The cluster \( Cl_0 \) includes \( (FF_0, FF_1, FF_2) \), and \( Cl_1 \) includes \( (FF_3, FF_4, FF_5) \). The cluster \( Cl_0 \) has the signature register \( SIG_0 \). The cluster \( Cl_1 \) has the signature register \( SIG_1 \). The clock line \( clk \) controls these flip flops. The control lines \( sc0[0] \) controls the capture operation of \( SIG_0 \), and \( sc0[1] \) controls the capture operation of \( SIG_1 \). The paths \( p_1, p_2, p_3, p_4 \) are sensitized simultaneously by the test vector \( (FF_0, FF_1, FF_2, FF_3, FF_4, FF_5) = (0,0,1,0,1,1) \). The test response of \( p_i \) is captured by \( FF_i \). The expected test response is \( (FF_0, FF_1, FF_2, FF_3, FF_4, FF_5) = (1,1,0,1,0,0) \).

The paths \( p_1 \) and \( p_2 \) are measured by \( SIG_0 \). The paths \( p_3 \) and \( p_4 \) are measured by \( SIG_1 \). The combination of the two paths, one of which is selected from \( p_1 \) and \( p_2 \), the other of which is selected from \( p_3 \) and \( p_4 \), can be measured simultaneously.
Although the four paths are sensitized by the test vector, two paths can be measured simultaneously at most. Hence, we measure the four paths divided into two measurement stages STG₀ and STG₁ each of which measures two paths simultaneously. Here, we measure p₁ and p₅ to STG₀ and SIG₁, respectively. STG₁—After each testing, send test responses of p₂ and p₃ to SIG₀ and SIG₁, respectively.

First, the test vector is set to the flip flops with scan-in operation. After that, the values of the flip flops are set to the extra latches (a). Second, the first stage measurement is performed (b). Third, the second stage measurement is performed (c). In each stage, the paths under measurement are tested multiple times with reducing the test clock width. Steps (b) and (c) show the state just after the test execution. The flip flops hold the test response. The latches hold the test vector. After the testing, the test responses are shifted to the signature registers SIG₀ and SIG₁ with the clock operation of clk. The required number of shift clocks of a stage is the maximum number of the shift clocks among the paths measured simultaneously in the stage. For example, in STG₀, two clocks are required to send the test response of p₁ to SIG₀, while one clock is required to send the test response of p₅ to SIG₁. Therefore the shift clocks of STG₀ are two clocks. Similarly the shift clocks of STG₁ are three clocks. Like this, the number of the required shift clocks varies in each stage. To capture only the target test response value, the control bit sequences are sent to sc₀ and sc₁. In SIG₀, the test response of p₁ is captured to FF₁. Therefore SIG₀ should capture the value two clocks later. This operation is realized by sending the bit sequence “01” to sc₀ synchronizing with the clk. To capture the test result of p₅, SIG₁ should capture the value one clock later. This operation is realized by sending the bit sequence “10” to sc₁ synchronizing to the clk in STG₀. In STG₁, the test response of p₂ is captured by sending the bit sequence “100” to sc₀, and the test response of p₃ is captured by sending the bit sequence “001” to sc₁, respectively.

Fig. 8 shows the timing chart of this operation. The low cost tester controls the whole measurement sequence. For the measurement both VCG clock and tester clock are used. The clock selection is controlled by cs. The trigger signal trg and the control signal c₁₀₉ is provided to VCG. The control data c₁₀₉ is updated after each testing operation. In STG₀, SIG₀ captures the test response in the second shift-out clock. Therefore sc₀ turns to 1 synchronizing with the negative edge of the first clock of the shift-out operation. The latch clock clk captures the values of the flip flops just after the scan-in operation is finished. The s₀₁, sₑ₁, sₑ are controlled as explained previously.

2) Whole Measurement Sequence: Here, we assume that the test set for the measurement TS has NTV test vectors t₁,…,tₙNTV−₁. The number of the stages of tᵢ is Nᵢ. Before measurement, we have to check if the flip flops, the latches, and the clock generator work correctly by applying test vectors or other checking methods. After that, the following measurement sequence is executed.

Step 1: Initialize the variable i = 0.
Step 2: If i is equal to NTV, finish, otherwise initialize the variable j to 0, and set pᵢ to the flip flops with scan-in operation.
Step 3: Send the values of the flop flops to the latches.
Step 4: The paths included in STGᵢ are measured simultaneously. After that, j is updated to (j + 1).
Step 5: If $j$ is equal to $N_{at(i)}$, go to Step 6, otherwise load the test vector from the latches to flip flops, and go to Step 4.

Step 6: $i$ is updated to $(i+1)$, and go to Step 2.

D. Tester Channel Reduction

If $sck$ of each signature register is directly fed to the inputs of the chip, it requires the same number of the extra inputs as the number of the signature registers. It increases tester channel width. To keep the tester channel width short, we use the BCD decoder as depicted in Fig. 6. The decoder circuit transforms $n$ bit binary code to the corresponding $2^n$ width decimal code. For example, when $n = 2$, $sck_0sck_1 = 01$, the corresponding decimal code is $sck_0sck_2sck_3 = 0100$. We explain how to encode the $sck$ bit sequences to the corresponding binary code $scj$ with the example depicted in Fig. 9. This example consists of three clusters $Cl_0$, $Cl_1$, and $Cl_2$. Each cluster has three flip flops. Consider the case that the test response of the sensitized paths are captured in $FF_{01}$, $FF_{12}$, $FF_{20}$. In the shift out operation after a testing, the test response of $FF_{01}$ is captured by $SIG_0$ two clocks later. Therefore the bit sequence “010” should be sent to $sck_0$. The test response of $FF_{12}$ is captured by $SIG_1$ one clock later. Therefore the bit sequence “100” should be sent to $sck_2$. The test response of $FF_{20}$ is captured by $SIG_2$ two clock later. Therefore the bit sequence “001” should be sent to $sck_2$. Each bit value of these bit sequences is grouped. The group of the 0th bit values is $sck_0sck_1sck_2 = 010$. Those of the first bit values and second bit values are $sck_0sck_2sck_3 = 100$, $sck_0sck_1sck_2 = 001$, respectively. We call each group slice. Here, $s_{d_i}$ represents the slice of $i$th bit. Finally, these decimal codes are transformed into the corresponding binary code. The 0th slice $s_{d_0} “010”$ is transformed to “01”. The 1st slice $s_{d_1} “100”$ is transformed to “10”. The second slice $s_{d_2} “001”$ is transformed to “11”. As a result, the bit width of the data is reduced from 3 bit to 2 bit by this transformation. Generally, the width of the slice of $sck$ is $n$, the width of encoded slice of $scj$ is $\lceil \log_2 n \rceil$. However, for the encoding, each slice is permitted only 1 bit with the value 1. More than two bits with value 1 is not permitted. This restriction puts the constrain on ATPG for the generation of the test set for the measurement.

E. Scheme for Decision of Number of Extra Latches

The proposed method uses extra latches to accelerate the measurement time. To simplify the explanation, we have assumed that each flip flop has an extra latch until the previous subsection. But adding an extra latch to each flip flop makes the area overhead unrealistic. To solve the problem, we make multiple flip flops share an extra latch.

This subsection explains the scheme for the decision of the number of the required extra latches. The proposed scheme decides the number of the required extra latches, the connection from the outputs of flip flops to the inputs of the latches, and the connections from the outputs of the latches to the latch lines of the flip flops. The proposed scheme makes the number of the required extra latches as small as possible considering the test vectors and the routing restriction. We explain the scheme with the example shown in Fig. 10. This example includes six proposed scan flip flops, $FF_{0} − FF_{5}$. The scan input and output are $sci$ and $sco$, respectively. All the paths are assumed to be measured by three test vectors, $tv_0 − tv_2$. A $X$ bit is represented by the symbol $X$. The bit vector $b_j = (b_{0j}, b_{1j}, b_{2j})$ is the set of the $j$th bits of the test vectors, where $b_{ij}$ is the $j$th bit of $tv_i$. Routing window is introduced to avoid extraordinary long redundant lines. In the process of searching the sets of flip flops sharing a latch, the search space is restricted within the window. In this example, the window width is three.

At first, the latch line of each flip flop is not connected. In phase (a), the routing window is set on the scan input. The bit vectors, $b_0$, $b_1$, $b_2$ of $FF_0$, $FF_1$, $FF_2$ inside the window are checked if there exists sets of bit vectors which are mergeable each other. If such a set exists, a latch is assigned to the set. The input of the latch is connected to the output of a flip flop of the set. The output of the latch is connected to the latch lines of all the flip flops of the set. In this example, $b_0$ and $b_1$ are mergeable. A latch $L_0$ is assigned. The merged bit vector is updated to the values after merge operation. The routing window is shifted 1 bit along the scan chain. The above operation is repeated until the routing window reaches the scan output in phases (b), (c), (d). After that, in the final phase (d), each flip flop whose latch line is not connected yet is assigned a latch, and the input is connected to the output of the flip flop, and the output is connected to the latch line.

F. Constraints for ATPG

The test set for the measurement is obtained by the deterministic test generation with ATPG. The measurement time depends on the sum of the number of the stages of the test vectors. Therefore, to reduce the stages of each test vector, we add the constraints to as many measure paths as possible.

Normal ATPG tries to sensitize paths in arbitrary order. However when the generated test set is applied to the measurement
the $sck$ of each signature register should meet the constraints explained in the previous subsection. Accordingly, the order of the path sensitization is determined by the sequence for the proposed measurement.

For the description of the sequence, we define some additional parameters and functions.

- $TS$: The obtained test set.
- $n(\text{max})_P$: The maximum number of paths measured by a test vector.
- $n(\text{max})_{STG}$: The maximum number of stage in each test vector.
- $FF(p)$: The end point of $p$.
- $N_c$: The number of clusters.
- $\text{existSensitizablePath}(v_i)$: If there exists any sensitizable paths left in the test vector $v_i$, return true, otherwise return false.
- $\text{isOccupiedCl}(j, p)$: During seeking paths for the $j$th stage, if there exists a path $p'$ that already assigned to $j$th stage and $FF(p)$ and $FF(p')$ is in the same cluster, return true, otherwise return false.
- $\text{isOccupiedLoc}(j, p)$: During seeking paths for the $j$th stage, if there exists a path $p'$ that already assigned to the $j$th stage and the orders of $FF(p)$ $FF(p')$ in each cluster are same, return true, otherwise return false.

The sequence is as follows.

**Step 1:** If all the paths are sensitized, finish, otherwise initialize $i = 0$, $j = 0$, $k = 0$, $l = 0$.

**Step 2:** If $\text{existSensitizablePath}(v_i)$ is false, or, $j$ is equal to $n(\text{max})_{STG}$, or $k$ is equal to $n(\text{max})_P$, push the test vector $v_i$ to $TS$, update $i = i + 1$, and go to Step 1, otherwise go to Step 3.

**Step 3:** If $l$ is equal to $N_c$, update $j = j + 1$, initialize $l = 0$, and go to Step 2, otherwise pick up a path $p$ from path list, and go to Step 4.

**Step 4:** If $\text{isOccupiedCl}(j, p)$ is true, go to Step 2, otherwise go to Step 5.

**Step 5:** If $\text{isOccupiedLoc}(j, p)$ is true, go to Step 2, otherwise go to Step 6.

**Step 6:** Try to sensitize $p$. If $p$ is sensitized successfully, assign $p$ to STG,$j$, and update $k = k + 1$, $l = l + 1$.

**G. Measurement Time and Data Volume**

We describe the measurement time and data volume. We assume that the test set $TS$ which has $N_{TV}$ test vectors,
The test data volume is $N_{TV}(L_{PI} + L_{PO} + L_{scan})$. The amount of the data indicating the polarity of the paths is $N_P$. The amount of data for control of the capture timing of the signature registers is $\log_2 N_{SIG} \times \sum_{i=0}^{N_{TV}-1} \sum_{j=0}^{N_{st}(i)-1} (1 + N_{shift}(ij))$. The amount of data for the signature register is $N_{meas} + 1) \log_2 N_{SIG}$. The amount of the data indicating the number of the measurement stages of each test vector is $N_{TV} \times [\log_2 N_{(max)st}]$, where $N_{(max)st}$ is the maximum number of the stages among $N_{st}(0), \ldots, N_{st}(N_{TV}-1)$. Therefore the $V_{SIG}$ is calculated by the following formula:

$$V_{SIG} = N_{TV}(L_{PI} + L_{PO} + L_{scan})$$

$$+ N_P + [\log_2 N_{SIG}]$$

$$\times \sum_{i=0}^{N_{TV}-1} \sum_{j=0}^{N_{st}(i)-1} (1 + N_{shift}(ij))$$

$$\times [N_{meas} + 1) \log_2 N_{SIG} + N_{TV}]$$

$$\times [\log_2 N_{(max)st}]$$

(4)

whereas the data volume for the measurement with normal scan design $V_{STD}$ is calculated by the following formula:

$$V_{STD} = N_{TV}(L_{PI} + L_{PO} + 2L_{scan})$$

(5)

### H. Test Response Tracing

The target paths of the proposed measurement are single-path sensitizable. However, some applications require lowest failing frequency [28], [29] and trace the test response sequence in a continuous sensitization of the path under measurement with reducing the test clock frequency.

In single-path sensitizable path measurement, it is guaranteed that once the test fails, the test with higher frequency than the failing frequency is fail.

But in single-path unsensitizable path measurement (for example, multiple reconvergent paths), it is not guaranteed. For example, in case of the example of Fig. 3, only the 6 patterns, “FFFFF”, “PPPPP”, “PPPPP”, “PPP”, “PPP”, “PPP” should be considered.

When a single-path unsensitizable path is measured, we could have responses such as “PPPPP”. For such a case, the proposed method has the test response tracing mode as an optional function. In this mode, the test response patterns are not compacted by signature registers. We get the raw test response pattern. This mode is realized by cutting off the feedback loop with sge = 0 during the measurement.

Let $L_{SIG}$ be the length of a signature register, then the measurement sequence of a path with the test response tracing mode is described as follows.

1. SIG is initialized.
2. Test vector is loaded from the latches.
3. Test clock width $T$ is set to normal clock width.
4. Test clock is applied.
5. The test response is sent to SIG with scan-out operation.
Step 6: If testing time is equal to \( N_{\text{timer}} \) or is multiple number of \( L_{\text{SIG}} \), the values of the flip flops of SIG is retrieved. After that, if testing time is equal to \( N_{\text{timer}} \), go to Step 7, otherwise go back to Step 2 after the test clock width \( T \) is updated to \( T = \Delta T \).

Step 7: The delay value is estimated by comparing the retrieved signature value and the signature table.

In this mode, we have to retrieve the values stored in the flip flops of the signature registers every \( L_{\text{SIG}} \) times. Therefore whole measurement time is longer than normal mode.

IV. EXPERIMENTAL RESULT

In this section, we present the experimental results. In Section IV-A, the proposed method is compared with the conventional methods.

The clock frequencies are the same as that of Noguchi’s methods [2], [4], that is, the normal clock frequency is 100 MHz, and the scan clock frequency is 10 MHz. The length of the signature register is 8 bit. The test set consists of test vectors which detects all single-path sensitizable transition faults. The paths sensitized by these test vectors are measured. In this evaluation, the average delay of signal propagation of the measured paths is assumed to be the half of the clock width. Usually the length of the sensitized paths for transition delay defect detection is relatively short because ATPG seeks the paths whose length is as short as possible for the cost of test generation. From this point of view, we believe that this assumption is valid. In this evaluation, the test set for the measurement is generated by podem-based ATPG algorithm, which is implemented by C++. The back track limit is 200. For the evaluation, relatively larger ISCAS’89 benchmark circuits are used.

The measurement time using the proposed scan design and standard scan design is calculated by the (1) and (3), respectively. The results of area are obtained by synthesis with Synopsys design compiler using Rohm 0.18 \( \mu \text{m} \) process. The data volume of these methods are calculated by the (4) and (5), respectively.

In this evaluation, area overhead \( O_A \), area overhead \( O_A' \) including the area of VCG, and the routing overhead \( O_R \) are defined as follows.

\[
O_A = (A/A_{\text{AMS}} - 1) \times 100.0, \quad O_A' = (A'/A_{\text{AMS}} - 1)\times 100.0, \quad O_R = (A_R/A_{\text{RMS}} - 1) \times 100.0,
\]

where \( A \) is the area of the circuits implemented the evaluated method except VCG, and \( A_{\text{AMS}} \) is the area of the non-scan circuit except clock generator. \( O_A' \) is the area of the circuits implemented the evaluated method including VCG. The area of VCG is obtained from the paper [11].

Note that \( A, A', A_{\text{AMS}} \) include the area of the wires. \( O_R = (A_R/A_{\text{RMS}} - 1) \times 100.0, \) where \( A_R \) and \( A_{\text{RMS}} \) are the routing area of the evaluated circuit and non-scan circuit, respectively.

The reduction ratio of measurement time \( R_T \) is defined as \( R_T = (1 - T/T_{\text{STD}}) \times 100.0, \) where \( T \) and \( T_{\text{STD}} \) is the measurement time of the evaluated method and that of standard scan, respectively.

The increase ratio of the data volume is defined as \( O_V = (V/V_{\text{STD}} - 1) \times 100.0, \) where \( V \) and \( V_{\text{STD}} \) is the data volume of the evaluated method and that of standard scan, respectively.

A. Comparison With Conventional Scan-Based Measurement

In this section, the proposed method is compared with the delay measurement with conventional scan designs, namely standard scan design and enhanced scan design. In this evaluation, \( n_{\text{MAX}} \) is fixed to 8. The length of cluster \( L_{CI} \) is restricted to 32 or 64.

1) Area Overhead: Table II shows the result of the area and routing overhead. The column circuit shows the name of benchmark circuits. The columns \( N_{\text{FF}} \) is the number of flip flops inside the circuit. The column \( A_{\text{MS}} \) is the area of the non-scan circuit (\( \text{mm}^2 \)). The columns STD, ENH, SIG show the evaluation results of the circuits applied standard scan, enhanced scan, and the proposed method, respectively. The subcolumn \( r_X \) is the number of the extra latches \( N_L \) against \( N_{\text{FF}} \), which is defined as \( r_L = N_L/N_{\text{FF}} \times 100.0 \). The difference between \( O_A \) of enhanced scan design and the proposed method is 7.4% on average. The difference is negligible considering the area overhead of standard scan design. The area overhead of the proposed method tends to decrease as the circuit’s size increases. One of the reasons is that \( r_L \) tends to decrease as the circuit’s size increases. According to the result, \( r_L \) tends to decrease as the \( X \) bit density is higher. The difference \( O_A \) of enhanced scan design and the proposed method of the larger circuits s38417 and s38584 are 2.8% and 4.2%, respectively. Because a test set of larger circuits has higher \( X \) bit density in general, the area overhead tends to be smaller as the size of the applied circuit increases. The area overhead of s35932 is larger in spite of the low \( X \) bit density. It is because the number of the signature registers is larger than those of s38417 and s38584 for the smaller \( L_{CI} \).

The same inclination can be seen in \( O_A' \) although the absolute value is larger for the area of VCG. The routing overhead \( O_R \) of the proposed method is 12.9% larger than that of enhanced scan design. But the impact to the whole area overhead \( O_A \) and \( O_A' \) is smaller.

2) Measurement Time: The result of the measurement time is shown in Table III. Here, we show the result when \( N_{\text{timer}} = 100 \) and \( N_{\text{timer}} = 200 \), respectively. The subcolumns \( T_{\text{STD}} \) (ms) and \( T_{\text{SIG}} \) (ms) are the measurement time of standard scan design and the proposed method, respectively. According to the result, \( R_T \) when \( N_{\text{timer}} = 100 \) and \( N_{\text{timer}} = 200 \) are 67.8% and 71.9%, respectively. The reduction ratio \( R_T \) when \( N_{\text{timer}} = 200 \) is 4.1% higher than \( R_T \) when \( N_{\text{timer}} = 100 \). It is because the impact of the time for scan-in operation of each test vector on the measurement time decreases as \( N_{\text{timer}} \) increases.

3) Data Volume: Table IV shows the evaluation result of the data volume and the reduction ratio when \( N_{\text{timer}} = 100 \) and \( N_{\text{timer}} = 200 \). The subcolumns \( V_{\text{STD}} \) (MBits) and \( V_{\text{SIG}} \) (MBits) are the data volume of standard scan design and the proposed method, respectively. The data volume when \( N_{\text{timer}} = 100 \) and when \( N_{\text{timer}} = 200 \) are 119.2% and 119.3% on average. They are almost the same. The larger \( N_{\text{timer}} \) is, the larger...
the amount data for the signature table. But the evaluation result shows that the impact on the whole data amount is negligible.

4) Estimation of Measurement Time of Larger Circuits: We estimate the measurement time of larger circuits. The scan chain length \(L_{\text{scan}}\) indicates the size of the circuits. Therefore we investigate the relation between \(L_{\text{scan}}\) and \(R_T\). When we assume that the number of the measured paths per a test vector is \(n_{\text{max}}\) and the distribution of the end points of the measured paths is uniform, the average of the number of the shift clock per a stage \(N_{\text{sft}}\) is approximated by the following formula, statistically:

\[
N_{\text{sft}} = \sum_{i=1}^{L_{\text{CL}}} i \left( \frac{i}{L_{\text{CL}}} \right)^{n_{\text{max}}} - \left( \frac{i}{L_{\text{CL}}} \right)^{n_{\text{max}}-1}.
\]

When \(L_{\text{CL}} = 64\) and \(n_{\text{max}} = 8\), \(N_{\text{sft}} = 574.4\). We assume \(k = 4.2\), which is the average value of Table II, and \(N_{\text{TV(standard)}} = 1000\).

Assuming these values, we calculate \(R_T\) when \(L_{\text{scan}} = 500, 1000, 3000, 5000, 10000\), and plot them. Fig. 11 shows the result. The horizontal axis is \(L_{\text{scan}}\). It indicates the size of the circuit. The vertical axis is \(R_T\). In this condition, \(R_T\) when \(L_{\text{scan}} = 500\) is negative value. However when \(L_{\text{scan}}\) is larger than 5000, it reaches to over 80%. The result shows that the proposed method gives better measurement time as the size of the circuits is larger.

Next, we investigate the influence of the variation of the number of the test vectors. The number of test vectors depends on the structure of circuits or ATPG algorithm. We plot the measurement time when \(N_{\text{TV(standard)}} = 500, 1000, 1500, 2000\) in the condition that \(L_{\text{scan}} = 5000\). Fig. 12 shows the result. The horizontal axis is \(N_{\text{TV(standard)}}\). The vertical axis is \(R_T\). As shown in this figure, the \(R_T\) increases as \(N_{\text{TV(standard)}}\) increases.

In this estimation, the interval between the adjacent signature registers is \(N_{\text{CI}} = 64\). Therefore the area overhead is in the same order of the previous evaluation. As the size of circuit increases, the influence of the area of the test clock generator on the area overhead is smaller. Therefore the area overhead will be convergent to that without the test clock generator.
B. Comparison With Delay Measurement Using Path Ring Oscillator

First, we compare the measurement time with the delay measurement method using path ring oscillator [21], [22]. They are compared under the condition of the experiment of [22] and referring the experimental result. The test clock frequency and the scan chain length of the target circuit is 100 (ns) and 100, respectively. The number of the paths under measurement is 100. The measurement time of both of [21] and [22] are the sum of the calibration time and the execution time of the measurement. According to [22], the calibration time of [21] and [22] are 700 and 17 μs, respectively. Here, the measurement time of the two methods are approximated with the time required for the scan-in operations of test vectors. Therefore the execution time of the measurement is approximated to 0.1 μs \times 100 \times 100 = 10000 \mu s.

The number of test vectors \(N_{TV}\) is set to the half of the number of the path \(N_{TV}\) considering those of the evaluated circuits of the same order. The length of the cluster \(L_{CI}\) is set to 10. The remaining parameters for the proposed methods are set to the same values of the previous evaluations. Table V shows the result. In this condition, the measurement time of the proposed method is 3.4 times of that of [21], 5.7 times of that of [22].

The area overhead is compared with [21] and [22] using b19, which is an ITC’99 benchmark circuit. Here, the area overhead of both for the proposed method \(O'_{A}^{m}\) is defined as \(O'_{A}^{m} = (A_{SIG}/A_{STD} - 1) \times 100\). It is compared with the results of [21] and [22] when the number of the path under measurement \(N_{PUL}\) is 50, 100, 200, 500. The set of paths under measurement for the proposed method is the one of the longest paths of randomly selected \(N_{PUL}\) end points. The length of cluster \(L_{CI}\) is set to 64. The other parameters are the same as the previous evaluations. Note that in this evaluation, the flip flops which are not assigned care bits are not connected to any extra latches.

Table VI shows the result. On average, the area overhead is 6.508% and 6.072% larger than those of [21] and [22], respectively.

C. Comparison With Delay Measurement Using Embedded Delay Measurement Circuit

Finally, the proposed method is compared with the delay measurement using embedded delay measurement circuits. In this evaluation, the architecture of the path measurement scheme proposed in [26] depicted in Fig. 13 is assumed. Table VII shows the result. The subcolumn EMB and SIG shows the evaluation results of the measurement using the embedded delay measurements and the proposed methods, respectively. The subcolumn \(r\) is the ratio of the delay measurement time of the proposed method against that of the measurement using embedded delay measurement. The area overhead of the proposed method is 8.2% larger on average. The value \(r\) is 1.4 on average. It means that the measurement time of the proposed method is 1.4 times of that of the embedded delay measurement approach. Actually the area overhead of the embedded delay measurement approach is area efficient. But it requires large-sized two multiplexes. Unless the layout and routing is performed carefully, it may give serious impact on the performance and measurement accuracy. On the other hand, the proposed method does not use the large-sized multiplexers but use scan chain and limited length extra wires. Therefore it has less probability of degradation of the performance of normal operation. The embedded delay measurement approach can measure a path per a test vector. Therefore the measurement time increases as the number of the measured path. In general, the measured path increases as the circuit size increases. Hence in the larger circuits like s38417 and s38584, the measurement time of the proposed method is better.

V. CONCLUSION

The proposals of this paper are as follows.

- The proposal of the delay measurement method using signature analysis and variable clock generator.
- The proposal of a scan design for the delay measurement of internal paths of SoC.
- The first proposal can be applied not only SoC but also field-programmable gate array (FPGA) [30]. Because the process of FPGA is getting extraordinary smaller these days, the small
delay defect becomes serious problem in FPGA, too. In this meaning, the application of the proposed method to FPGA is also useful. A future work is the low cost application of the proposed measurement to FPGA.

When we measure short paths the measurement error can increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction of the test quality. Another future work is the low cost application of the proposed method to FPGA is also useful. A future work is the low cost application of the proposed method to FPGA.

APPENDIX

The signature value of a rising transition testing can be calculated from the corresponding one of falling transition testing, and vice versa. Let $\text{sig}_{\text{ri}}$ be the signature value of the rising transition of Case $i$, and let $\text{sig}_{\text{fi}}$ be that of the falling transition: then

$$\text{sig}_{\text{ri}} \oplus \text{sig}(111111) = \text{sig}_{\text{fi}}$$

(6)

where $\text{sig}(b_0 \cdots b_{n-1})$ is the signature value when the $n$ bit binary sequence $b_0 \cdots b_{n-1}$ is sent to the signature register.

The reason is as follows. Linearity of the signature value gives the following relation between the two bit sequences $b_{r\text{ri}} \cdots b_{r(i-1)}$ and $b_{f\text{ri}} \cdots b_{f(i-1)}$

$$\text{sig}(b_{r\text{ri}} \cdots b_{r(i-1)} \oplus \text{sig}(111111)) = \text{sig}(b_{r\text{ri}} \cdots b_{r(i-1)} \oplus b_{f\text{ri}} \cdots b_{f(i-1)},$$

Substitute $111111$ for $b_{r\text{ri}} \cdots b_{r(i-1)}$: then

$$\text{sig}(b_{r\text{ri}} \cdots b_{r(i-1)} \oplus \text{sig}(111111)) = \text{sig}(b_{r\text{ri}} \cdots b_{r(i-1)} \oplus 111111).$$

(7)

Let $b_{r\text{ri}} \cdots b_{r(i-1)}$ and $b_{f\text{ri}} \cdots b_{f(i-1)}$ be the test response sequences of the rising and falling transition test of Case $i$, respectively: then

$$b_{r\text{ri}} \cdots b_{r(i-1)} \oplus 111111 = b_{f\text{ri}} \cdots b_{f(i-1)},$$

(8)

Substitution of (8) into (7) gives (6).

Therefore the amount of the data for the signature table of (4) is not $2(N_{\text{dels}} + 1) L_{\text{sig}}$ but $(N_{\text{dels}} + 1) L_{\text{sig}}$.

REFERENCES


Kentaroh Katoh (M’04) received the B.E. and M.E. degrees from Nagoya University, Nagoya, Japan, in 1997 and 1999, respectively, and the Ph.D. degree from Chiba University, Chiba, Japan, in 2009.

In 1999, he joined Fujitsu Limited and engaged in the development of the embedded control system of HDD from 1999 to 2001. He joined Chiba University, in 2001. Since 2011, he has been a member of Tsuruoka National College of Technology. He is currently an Associate Professor with the Electrical Engineering Department. His research interests include testing method and fault-tolerant design of reconfigurable hardware and SoC. He is a member of the IEICE.

Kazuteru Namba (M’03) received the B.E., M.E., and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1997, 1999, and 2002, respectively.

He joined Chiba University, Chiba, Japan, in 2002. He is currently an Assistant Professor with the Graduate School of Advanced Integration Science, Chiba University. His current research interests include dependable computing.

Dr. Namba is a member of the IEICE and the IPSJ.

Hideo Ito (M’01) was born in Chiba, Japan, on June 1, 1946. He received the B.E. degree from Chiba University, Chiba, Japan, in 1969 and the D.E. degree from Tokyo Institute of Technology, Tokyo, Japan, in 1984.

He joined Nippon Electric Co. Ltd. in 1969 and Kisarazu Technical College in 1971. Since 1973, he has been a member of Chiba University. He is currently a Professor of Graduate School of Advanced Integration Science. His research interests include easily testable VLSI design, defect-tolerant computing, and dependable computing.

He is a fellow of the IEICE and a member of the IPSJ.