

# On-Chip Measurement and Compensation of Timing Imbalances in High-Speed Serial NoC Links

*Sebastian Höppner, Technische Universität Dresden, Dresden, Germany*

*Dennis Walter, Technische Universität Dresden, Dresden, Germany*

*Georg Ellguth, Technische Universität Dresden, Dresden, Germany*

*René Schüffny, Technische Universität Dresden, Dresden, Germany*

---

## ABSTRACT

*This paper presents techniques for measurement and compensation of timing variations in clock and data channels of source-synchronous high-speed serial network-on-chip (NoC) links. Timing mismatch measurements are performed by means of asynchronous sub-sampling. This allows the use of low quality sampling clocks to reduce test hardware overhead for integration into complex MPSoCs (Multiprocessor System-on-Chip) with multiple NoC links. The effect of clock jitter on the measurement results is evaluated. Delay mismatch is compensated by tunable delay cells. The proposed technique enables compensation of delay variations to realize high-speed NoC links with sufficient yield. It is demonstrated at NoC links as part of an MPSoC in 65 nm Complementary Metal Oxide Semiconductor technology, where the calibration significantly reduces bit-error-rates of a 72 GBit/s (8 GBit/s per lane) link over 4 mm on-chip interconnect.*

*Keywords: All Digital Phased-Locked Loops, Asynchronous Sub-Sampling, Complementary Metal–Oxide–Semiconductor (CMOS), Delay Cell, Globally Asynchronous Locally Synchronous (GALS), Jitter, Mismatch, Multiprocessor System-On-Chip (MPSoC), Network-on-Chip (NoC), On-Chip Communication*

---

## INTRODUCTION

High-speed serial point to point connections are proven to be energy and area efficient solutions for on-chip data transmissions over long

distances in the range of some mm in networks-on-chip (NoCs) (Mensink et al., 2010; Walter et al., 2012). Although conventional 2D-mesh NoC topologies require only shorter point to point links between adjacent cores, the proposed long distance interconnects can enable efficient implementation of advanced NoC topologies like for example hierarchical 2D-mesh NoCs

DOI: 10.4018/jertcs.2012100103

(Winter et al., 2010), where higher layer point-to-point links bridge distances over multiple cores. As link data rates increase, the influence of process variations gets more severe especially in sub-100nm CMOS technologies. To achieve high data rates and maximize yield, calibration techniques have to be employed to compensate static mismatch variations. In Höppner et al. (2010) a calibration strategy with optimal sizing of compensation delay elements has been proposed. However, measurement access to on-chip signal characteristics is required. Asynchronous sub-sampling, where a high-speed signal is periodically sampled by a low-speed clock, is widely used for on-chip measurement purposes. In Schaub et al. (2008) on-chip oscilloscopes using asynchronous sampling clocks are presented which allow measurement of high-speed signals but require low jitter sampling clocks. This is a major drawback for complex MPSoCs where measurement signals have to be distributed over longer distances with negligible circuit and area overhead. In Amrutur et al. (2010) measurement of static skews of periodic signals is proposed using statistical averaging. This approach eases integration due to relaxed requirements for sample clock qual-

ity. Using this method periodic on-chip signals whose period is in the range of sample clock jitter can be characterized.

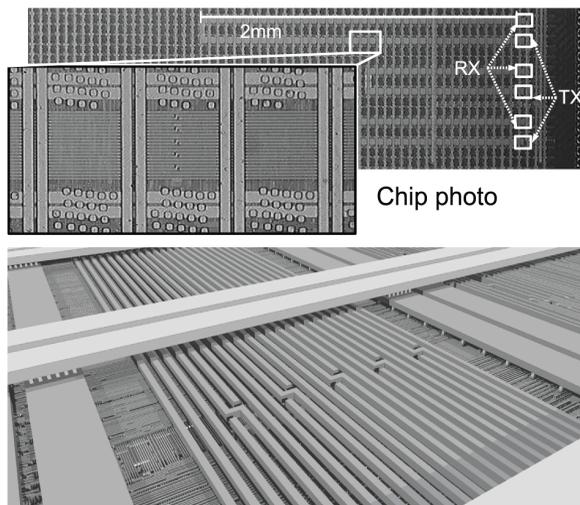
This work presents an asynchronous sub-sampling technique (Höppner et al., 2011) to provide measurement access to delay characteristics of multiple high-speed NoC links in a 65 nm MPSoC. Therefore, a low frequency asynchronous sampling clock with relaxed jitter requirements can be used which simplifies integration and scalability.

## NOC LINK ARCHITECTURE

### Overview

We consider MPSoC network-on-chip point-to-point connections over large distances (e.g., some mm) as shown in Figure 1. Data is transmitted differentially with low voltage swing to achieve high energy efficiency. The link architecture shown in Figure 2 uses high speed serialization and deserialization (SERDES) where each NoC link contains a single high-speed clock lane and several data lanes with a serialization factor  $m$ . Each lane consists of two differential lines. The clock is shifted by  $90^\circ$  at

*Figure 1. High-speed NoC links routed in the upper metal layers between power mesh of MPSoC in 65 nm CMOS*



13 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the product's webpage:

[www.igi-global.com/article/chip-measurement-compensation-timing-imbalances/74343?camid=4v1](http://www.igi-global.com/article/chip-measurement-compensation-timing-imbalances/74343?camid=4v1)

This title is available in InfoSci-Journals, InfoSci-Journal Disciplines Communications and Social Science.

Recommend this product to your librarian:

[www.igi-global.com/e-resources/library-recommendation/?id=2](http://www.igi-global.com/e-resources/library-recommendation/?id=2)

## Related Content

---

### Managerial Issues for Telecommuting

Anthony R. Hendrickson and Troy J. Strader (2006). *Cases on Telecommunications and Networking* (pp. 77-89).

[www.igi-global.com/chapter/managerial-issues-telecommuting/6456?camid=4v1a](http://www.igi-global.com/chapter/managerial-issues-telecommuting/6456?camid=4v1a)

### Recent Advances and Challenges in Wireless QoE-Aware Multimedia Streaming Systems

Rosinei Oliveira, Ádamo L. Santana, João C. W. A. Costa, Carlos R. L. Frances, Elisangela Aguiar, Paulo Bezerra, Allan Costa, Eduardo Cerqueira and Antônio J. G. Abelém (2012). *Multimedia Services and Streaming for Mobile Devices: Challenges and Innovations* (pp. 224-243).

[www.igi-global.com/chapter/recent-advances-challenges-wireless-qoe/58706?camid=4v1a](http://www.igi-global.com/chapter/recent-advances-challenges-wireless-qoe/58706?camid=4v1a)

### Fractal Geometry and Computer Science

Nicoletta Sala (2009). *Selected Readings on Telecommunications and Networking* (pp. 385-404).

[www.igi-global.com/chapter/fractal-geometry-computer-science/28736?camid=4v1a](http://www.igi-global.com/chapter/fractal-geometry-computer-science/28736?camid=4v1a)

## How Recession and the Empowerment of Consumers Impact the Telecommunications Industry: A European Perspective

Bob Fox and Rob van den Dam (2012). *International Journal of Interdisciplinary Telecommunications and Networking* (pp. 38-47).

[www.igi-global.com/article/recession-empowerment-consumers-impact-telecommunications/67576?camid=4v1a](http://www.igi-global.com/article/recession-empowerment-consumers-impact-telecommunications/67576?camid=4v1a)