ECS Journal of Solid State Science and Technology, **6** (4) P197-P200 (2017)

A Wafer-Scale Ni-Salicide Contact Technology on n-Type 4H-SiC

Hossein Elahipanah,[z] Ali Asadollahi, Mattias Ekström, Arash Salemi, Carl-Mikael Zetterling, and Mikael Östling

School of Information and Communication Technology, KTH Royal Institute of Technology, Kista SE-164 40, Sweden

A self-aligned Nickel (Ni) silicide process (Salicide) for n-type ohmic contacts on 4H-SiC is demonstrated and electrically verified in a wafer-scale device process. The key point is to anneal the contacts in two steps. The process is successfully employed on wafer-level and a contact resistivity below $5 \times 10^{-6}\ \Omega \cdot cm^2$ is achieved. The influence of the proposed process on the oxide quality is investigated and no significant effect is observed. The proposed self-aligned technology eliminates the undesirable effects of the lift-off process. Moreover, it is simple, fast, and manufacturable at wafer-scale which saves time and cost.
© The Author(s) 2017. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0041705jss] All rights reserved.

Manuscript submitted January 23, 2017; revised manuscript received February 21, 2017. Published March 3, 2017.

Silicon carbide (SiC) is a well-known wide bandgap semiconductor for high temperature and high power applications due to its unique electrical and physical properties.[1–4] The self-aligned silicide process (Salicide) has been developed in Si technology for many years.[5,6] The two-step annealing silicide process has been widely known and used in silicon CMOS technology since the 1980s.[5,6] The Ti- and Co-based Salicide processes in silicon CMOS used two-step processing specifically to reduce the resistivity of the contacts ($\Omega \cdot cm$).[5,6] In spite of this progress, unlike the Si technology, forming a good ohmic contact to SiC is a persistent problem which requires high temperature annealing ($\sim$1000°C).[1] The two-step annealing has been previously used for SiC technology to form Co-based contacts to n-type[7–9] and for Ni-Al contacts to p-type.[10] However, it should be noted that the two-step annealing has been used to initiate reactions at lower temperatures. To the best of our knowledge, two-step annealing for the self-alignment process has not been presented in SiC device technology though some studies have been reported on self-aligned process in some type of devices.[11–15] Nickel (Ni) silicide is shown to be a good choice for the n-type ohmic contacts.[16–21] For SiC, Ni_2Si is rectifying until annealed at 950°C, without any obvious phase-change. The Ni layer cannot be patterned by reactive ion etching (RIE). Therefore, the lift-off process, wet etching, or ion milling of Ni become alternatives for Ni etching. The lift-off process, which is widely used to form the metal stacks, requires a thick photoresist layer that limits the downscaling and leaves metal residues and jagged metal edges. Therefore, it is desirable to avoid using lift-off process for wafer-scale industrial applications. SiC contact technology suffers from the lack of a simple and clean self-aligned Ni process particularly on wafer-scale. Moreover, downscaling of SiC-based devices and circuits is hampered by a lack of reliable self-aligned process to form the metal contacts and short channels.[1] High temperature annealing of metal/SiO_2 increases the risk of diffusion-reaction of metal and oxide layer which could affect large area devices and circuits functionality. Also, the quality of silicide surface and coverage significantly affects the device behavior.

In this work, a wafer-scale self-aligned n-contact with a two-step rapid thermal annealing (RTA) is demonstrated. The electrical and physical properties of the contacts are studied. The key point is to perform a first step annealing (FSA) of Ni layer at low-temperature (550–700°C) to form one phase of Ni_ySi_x and removing the unreacted Ni by a selective wet etch in Piranha ($H_2SO_4 + H_2O_2$ (3:1)). Afterward, the second step annealing (SSA) at high temperature (950°C) produces a low contact resistance. This eliminates the effect of high temperature annealing of Ni/SiO_2 layer which could affect the quality of oxide at higher temperatures. This method is successfully employed on a 4-inch SiC wafer process and the surface quality and the coverage of silicide in the oxide openings is significantly improved in comparison with the lift-off process. This method improves the yield and reduces the process complexity. Unlike the lift-off process, the thin oxide opening could simply be shrunk, filled in by the sputtered metal and annealed to form the contact. Also, no underlap is required in the contact openings which improves the silicide coverage. The proposed self-aligned technology could widely be used for all kind of SiC devices and integrated circuits to form the n-type ohmic contacts.

Experimental

N-type 4-inch 4H-SiC wafers with the doping of $>1 \times 10^{19}\ cm^{-3}$ are used in our investigation. The wafer surface is cleaned in Piranha, HF:H_2O, and the RCA baths to remove the organic contaminant and the native oxide. A 100-nm layer of SiO_2 is conformally formed at 350°C on the surface of the SiC samples and the contact windows are opened by dry etching process. An O_2 cleaning for 10 minutes and conditioning process for 10 minutes are consequently done in the oxide deposition chamber, which significantly improves the oxide quality and uniformity. A 100-nm Ni layer is sputtered using a pre-sputtering process. The pre-sputtering is done for 20 sec on the wafer to remove the possible formed oxide at the SiC surface and on the Ni target to remove any contamination from the target. Fig. 1 presents the process step flow and annealing profile of the self-aligned n-contact. The FSA is performed to form one phase of Ni silicide in the contact openings. Temperature steps from 450 to 1000°C in N_2 ambient to find the optimum temperature of the FSA are performed. To protect the formed silicide and the Ni layer from oxidation after the annealing steps, a continuous purging with N_2 for 3 minutes is done in the chamber to cool down the wafer to below 200°C before unloading the wafer. Then, the sample is dipped into the Piranha to remove the unreacted Ni. The SSA at 950°C for 1 min in N_2 ambient to form the low-resistivity ohmic contacts is performed. The contact

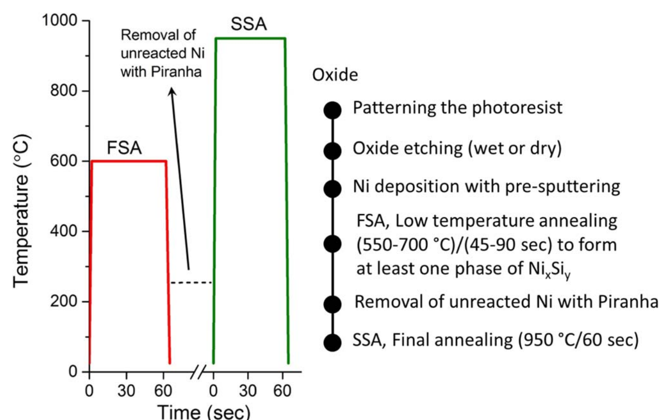

Figure 1. (Left) the schematic annealing profile and (right) the process step flow of the self-aligned process on n-type 4H-SiC.

[z]E-mail: hosseine@kth.se

Downloaded on 2017-03-03 to IP 130.237.29.138 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

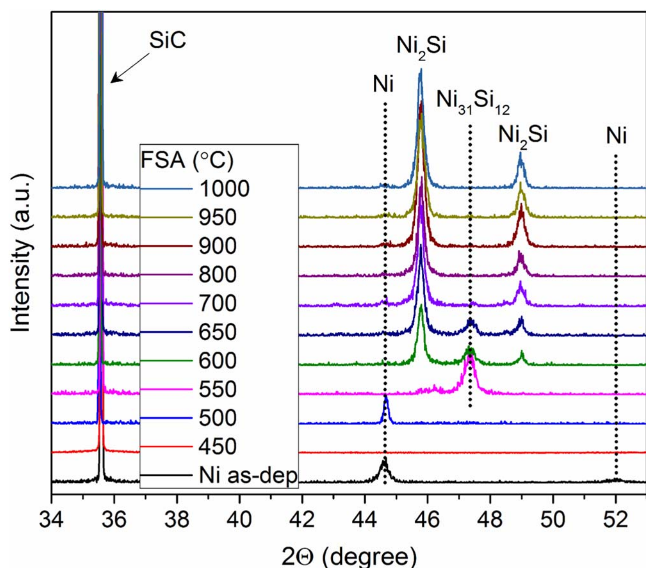

Figure 2. The XRD spectra of the Ni contact layer after the first step annealing (FSA) at different temperatures and removal of unreacted Ni.

characteristics as a function of the annealing temperature profiles are evaluated in terms of electrical and structural properties. In order to measure the contact resistivity (ρ_C), linear transmission line model (TLM) structures with rectangular pads with spacing from 5 μm to 25 μm are fabricated. Finally, 1-μm Al/TiW was sputtered and patterned to form the final metal pads. For further investigation, the structural analyses at the interface of Ni/4H-SiC and the formation of Ni_xSi_y silicide phases by X-ray diffraction (XRD) are done. The morphology of the contacts by atomic-force microscopy (AFM) is studied.

Results and Discussion

The proposed self-aligned process is based on two annealing steps. The formation of Ni-silicide (Ni_xSi_y) compounds is an important factor to form a low-resistive electrical contact between Ni and 4H-SiC.[16–21] The silicide phase at the Ni/4H-SiC interface changes at different annealing temperature. To find the optimum temperature range of the FSA, the formation of Ni_xSi_y silicide at different temperatures is investigated by XRD. Fig. 2 presents the XRD spectra of the Ni silicide contacts after the FSA at different temperatures. A 4H-SiC reference and an as-deposited Ni sample are also added as references in which a peak of single-crystaline 4H-SiC and poly-crystalline Ni are visible. A phase transformation of Ni-silicide is obvious for different annealing temperatures. This interaction between Ni and Si is the key point in this self-aligned process that allows the following wet removal of the unreacted Ni and the consequent SSA. $Ni_{31}Si_{12}$ at below 600°C and Ni_2Si for higher temperatures are the main phases while no trace of Ni is observed after the FSA and removal of unreacted Ni. The SSA at 950°C is necessary to produces low-resistive ohmic contacts.[16–20] The silicide formation starts at 550°C and its phase transformation continues at higher temperatures. The intensity of the Ni_2Si peak is dramatically increased at above 700°C. The contact surface became rougher at higher annealing temperatures. Due to presence of Ni atoms, different phases of Ni_xSi_y could be formed due to diffusion and reaction of these atoms. The silicide starts to agglomerate when the temperature increases and the silicide islands become visible. The AFM images of the samples after FSA and wet removal step and after the SSA at 950°C compared with the as-deposited Ni are shown in Fig. 3. The annealing process influences the surface morphology of the samples which is attributed to the reaction of Ni and Si and the phase transformation of Ni-silicide. The short annealing time in RTA and the thickness of Ni film could affect the formation of the silicide and its morphology.[21] The formation of silicide in larger areas is much more uniform than in the smaller openings. This might be attributed to the immediate expansion of the Ni layer surrounded by oxide sidewalls during the RTA process. The annealing process affects the quality of oxide which could be a passivation layer of BJTs,[3,4] gate oxide of MOSFETs,[11,12] side-wall oxide of JFETs and trench devices,[13] etc. Fig. 4 illustrates the scanning electron microscopy (SEM) image of the Ni-contacts formed by the lift-off process and the double-step annealing salicide process. The contact with lift-off has metal residues and jagged edges whereas the one with the silicide process has smooth metal edges and clean oxide surface.

Fig. 5 presents the *I-V* electrical characteristic of the Ni contacts after the FSA from 450 to 950°C. The typical Schottky behavior of the

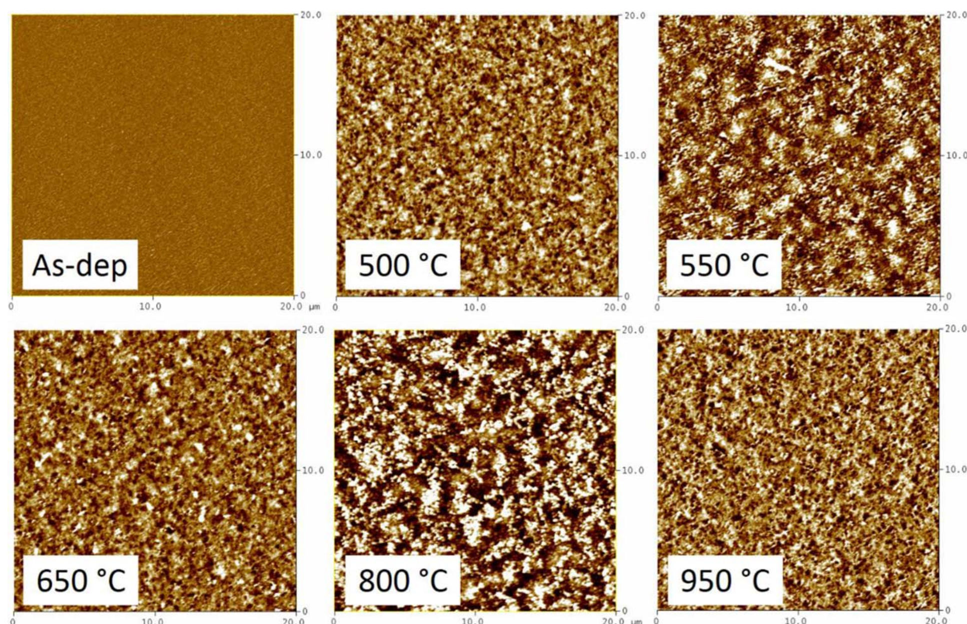

Figure 3. The AFM images of the silicide contact surface after removal of the unreacted nickel at different temperatures of the FSA. The AFM scanning size is $20 \times 20\ \mu m^2$.

Downloaded on 2017-03-03 to IP 130.237.29.138 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

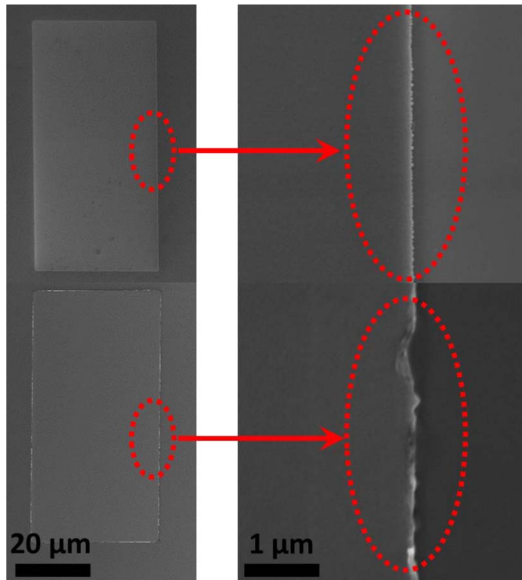

Figure 4. The SEM images of Ni n-contacts on 4H-SiC formed by (bottom) lift-off and (top) salicide process. The proposed Ni-salicide technology results in a smoother metal edge and cleaner oxide surface.

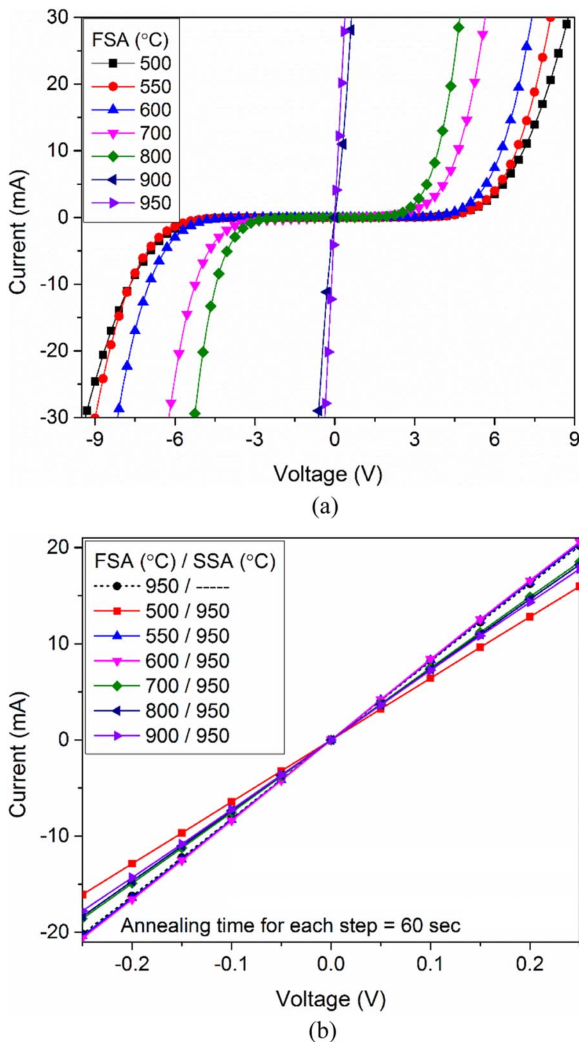

Figure 5. The *I-V* characteristic of the Ni contacts (a) after the FSA at different temperatures and removal of unreacted Ni and (b) after the SSA at 950°C. All samples with FSA > 500°C become ohmic after the SSA at 950°C.

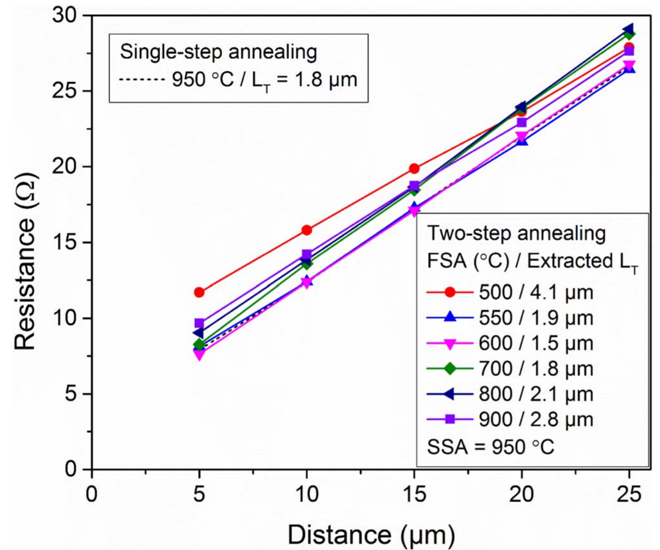

Figure 6. The total resistance measured for the TLM structures with different pad distances at various FSA temperatures 500 to 900°C followed by the SSA temperature at 950°C. The transfer length (L_T) is extracted for each sample.

contacts at lower annealing temperatures gradually changes to ohmic behavior at higher annealing temperatures. All samples with FSA > 500°C become ohmic after the SSA at 950°C. However, the lower annealing temperature of Ni/SiO_2 saves the oxide quality. The FSA range between 550 to 700°C results in low-resistive ohmic behavior after the SSA at 950°C. It is also found that the annealing time between 45–90 seconds is sufficient for the FSA and SSA steps. Hence, the proposed two-step self-aligned process benefits from a wide process window for the annealing temperature and time which makes it a reliable contact technology. The influence of the proposed process on the oxide quality is optically and electrically investigated and no significant effect is observed.

The TLM plots with different FSA temperatures and SSA at 950°C are shown in Fig. 6. To fairly measure the contact characteristics, the total resistance of different samples is calculated by differentiation of the *I-V* curves for different distances of TLM pads. All samples with FSA > 500°C shows ρ_C below $1 \times 10^{-5}\ \Omega \cdot cm^2$ whereas the samples with the FSA in the range of 550 to 700°C shows ρ_C below $5 \times 10^{-6}\ \Omega \cdot cm^2$ which is comparable to that of the conventional single-step annealing at 950°C. It should be noted that the difference between contact resistances is mainly attributed to the doping variation of the samples. As mentioned earlier, the ρ_C decreases for higher annealing temperatures of FSA. The wafer mapping of the measured contact resistivity is shown in Fig. 7. Among the 112 measured dies with TLM structures, above 50% has a contact resistivity below $5 \times 10^{-6}\ \Omega \cdot cm^2$ and more than 80% has a contact resistivity below $6 \times 10^{-6}\ \Omega \cdot cm^2$. A high uniformity for the contact resistivity is achieved.

Conclusions

A self-aligned Nickel (Ni) silicide process (Salicide) for n-type ohmic contacts on 4H-SiC is demonstrated and electrically verified on wafer-scale and a high uniformity for the contact resistivity is achieved. To avoid the undesirable effect of the high temperature annealing of Ni/SiO_2, the annealing is performed in two steps. A first step annealing (FSA) at low temperature is performed to form one phase of Ni_xSi_y and the unreacted Ni on SiO_2 is removed by Piranha. The second step annealing (SSA) at 950°C to form the low-resistance n-type ohmic contacts is then performed. It is found that the FSA range at 550–700°C with the duration of 45–90 seconds results in a contact resistivity below $5 \times 10^{-6}\ \Omega \cdot cm^2$ which is comparable to the conventional silicide formation at 950°C. The proposed self-aligned

Downloaded on 2017-03-03 to IP 130.237.29.138 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

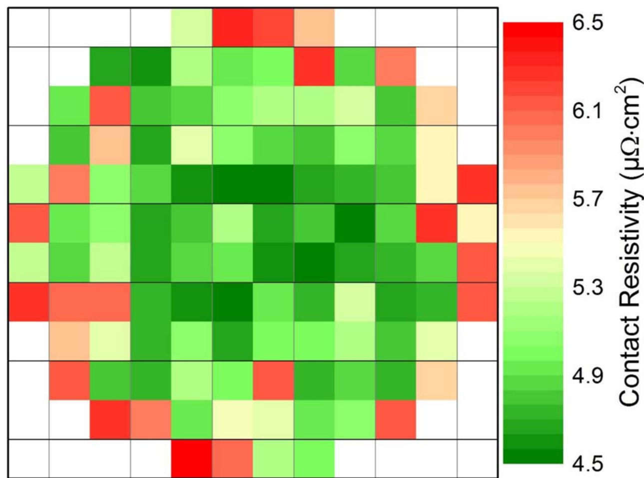

Figure 7. The wafer mapping of the measured contact resistivity on the wafer with 112 dies.

process eliminates the undesirable effects of the high temperature annealing of Ni/SiO_2 and lift-off process. Moreover, it is simple, fast, and manufacturable at wafer-scale which saves time and cost.

References

1. C.-M. Zetterling, *Process Technology for Silicon Carbide Devices*. London, U.K.: IET, Mar. 2002.
2. T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*. Singapore: Wiley, 2014.
3. M. Östling, R. Ghandi, and C.-M. Zetterling, "SiC power devices—Present status, applications and future perspective," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, May 2011, pp. 10–15.
4. H. Elahipanah, A. Salemi, C.-M. Zetterling, and M. Östling, "5.8-kV implantation-free 4H-SiC BJT with multiple-shallow-trench junction termination extension," *IEEE Electron Dev. Lett.*, **36**(2), 168 (2015).
5. S. L. Zhang and M. Östling, "Metal silicides in CMOS technology: past, present, and future trends," *Critical Rev. in Solid State Mat. Sci.*, **28**(1), 1 (2003).
6. C. K. Lau, Y. C. See, D. B. Scott, J. M. Bridges, S. M. Perna, and R. D. Davies, "Titanium disilicide self aligned source/drain + gate technology," in *IEDM*, 1982.
7. N. Lundberg and M. Östling, "$CoSi_2$ ohmic contacts to n-Type 6H-SiC," *Solid-State Electron.*, **38**(12), 2023 (1995).
8. N.-I. Cho, K.-H. Jung, and Y. Choi, "Improved ohmic contact to the n-type 4H-SiC semiconductor using cobalt silicides," *Semicond. Sci. Technol.*, **19**(3), 306 (2003).
9. K. Smedfors, C.-M. Zetterling, and M. Östling, "Sputtered ohmic cobalt silicide contacts to 4H-SiC," *Mat. Sci. Forum*, **821–823**, 440 (2015).
10. H. Vang, M. Lazar, P. Brosselard, C. Raynaud, P. Cremillieu, J.-L. Leclercq, J.-M. Bluet, S. Scharnholz, and D. Planson, "Ni-Al ohmic contact to p-type 4H-SiC," *Superlattices Microstructures*, **40**(4–6), 626 (2006).
11. M. Matin, A. Saha, and J. A. Cooper, "A self-aligned process for high voltage, short-channel vertical DMOSFETs in 4H-SiC," *IEEE Trans. Electron Dev.*, **51**(10), 1721 (2004).
12. J. A. Cooper and A. Agarwal, "SiC power switching devices - the second electronics revolution," *Proc. IEEE*, **90**(6), 956 (2002).
13. S. R. Wang and J. Cooper, "Double-self-aligned short-channel power DMOSFETs in 4H-SiC," in *Dev. Res. Conf.*, CA, USA, Jun. 2009, pp. 277–278.
14. K. Zekentes, A. Stavrinidis, G. Konstantinidis, M. Kayambaki, K. Vamvoukakis, E. Vassakis, K. Vasilevskiy, A. B. Horsfall, N. G. Wright, P. Brosselard, S. Q. Niu, M. Lazar, D. Planson, D. Tournier, N. Camara, and M. Bucher, "4H-SiC VJFETs with self-Aligned contacts," *Mat. Sci. Forum*, **821-823**, 793 (2015).
15. K. Vassilevski, I. Nikitina, A. B. Horsfall, N. G. Wright, A. J. Smith, and C. M. Johnson, "Silicon carbide vertical JFET with self-aligned nickel silicide contacts," *Mat. Sci. Forum*, **679-680**, 670 (2015).
16. Y. Jung and J. Kim, "Formation of Ni-silicide at the interface of Ni/4H-SiC," *J. Electrochemical Soc.*, **158**(5), H551 (2011).
17. S. Cichoň, P. Macháč, B. Barda, V. Machovič, and P. Slepička, "Raman study of Ni and Ni silicide contacts on 4H– and 6H–SiC," *Thin Solid Films*, **520**(13), 4378 (2012).
18. A. Kuchuk, V. Kladko, M. Guziewicz, A. Piotrowska, R. Minikayev, A. Stonert, and R. Ratajczak, "Fabrication and characterization of nickel silicide ohmic contacts to n-type 4H Silicon Carbide," *J. Phys.: Conf. Series*, **100**(4), 1 (2008).
19. Y. Cao and L. Nyborg, *Properties and Applications of Silicon Carbide*. Singapore: Wiley, 2011. ch. 8.
20. K. Smedfors, L. Lanni, M. Östling, and C.-M. Zetterling, "Characterization of ohmic Ni/Ti/Al and Ni contacts to 4H-SiC from −40°C to 500°C," *Mat. Sci. Forum*, **778–780**, 681 (2014).

Downloaded on 2017-03-03 to IP 130.237.29.138 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).