From the EIC

3D Test

We start the new year where we left the previous one: on test. This is also a continuation of our intense focus on 3-D circuits after a couple of special issues on that topic in 2016 showing the open challenges on testing 3-D designs. My thanks go to Guest Editors Erik Jan Marinissen and Yervant Zorian for bringing this important issue to the *IEEE Design&Test* magazine.

Our section of General Interest coverage has four papers. EDA for analog circuits remains a challenge as it faces many open issues. In "Estimating the Impact of Methodology on Analog Integrated Circuit Design Time," Jalas and Rahkonen discuss how far the time-to-market is influenced by the chosen design methodology. It is a fact that design methodologies for analog circuits vary greatly compared to design methodology for digital designs. As a result of their investigations, the authors suggest to maintain the required design methodology even though it might impose a higher risk.

In "Soft Error Mitigation Using Transmission Gate With Varying Gate and Body Bias," Sayil et al. deal with the soft error problem that increases with advanced technology modes. The authors therefore propose to adjust the gate voltages as well as body biases of individual pass transistors on the transmission gates along with additional techniques and finally achieve a considerable area saving compared to the state of the art.

A hardly explored problem is the interdependency between testability and security. It appears that both represent conflicting goals since testability requires deep insight while security suggests the opposite. In "A Comprehensive Design-for-Test Infrastructure in the Context of Security-Critical Applications," Saeed and Sinanoglu propose techniques showing that testability and security can be accomplished in an orthogonal manner.

In "Test Generation Methods for Utilization Improvement of Hardware-Accelerated Simulation Platforms," Kadry et al. focus on the problem of test generation for hardware-accelerator platforms used instead of software-based simulation. The goal is to increase their utilization to speed up the validation time. In fact, the authors report an improvement of 7×.

Turning to our Departments, Magdy Abadir, one of our Interview Editors, brings us one of the highlights of this issue: an interview with Wally Rhines, Chief Executive Officer of Mentor Graphics.

A further highlight is the Perspective from Mark Papermaster, Chief Technology Officer from AMD, who gives us insight on how to develop products for the immersive computing era.

As embedded systems grow more complex and as new applications such as the Internet of Things (IoT) require many design constraints, sophisticated design space exploration techniques are essential to find the best compromise between different design goals and their tradeoff. The Tutorial by Andy Pimentel gives a structured insight into the field of design space exploration for embedded systems.

Our coverage of conferences in this issue of *IEEE Design&Test* is on the IEEE/ACM Embedded Systems Week (ESWEEK) that took place in October 2016 in Pittsburgh, PA and is presented here by the conference's General Chairs.

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Last but not least we also include the Last Byte from Scott Davidson titled “Research Is Its Own reward.”

We are proud to announce that *IEEE Design&Test* is now printed fully in color, which should provide the readers with an enhanced experience. This shift also involves the availability of the electronic version that is complemented with a so-called digital screen version. Hence, *IEEE Design&Test* can be viewed on smartphones, notebooks, and other computer screens, simulating the printed version of the magazine. Many thanks go to the IEEE CEDA’s (Council on Electronic Design Automation) Vice President of publications Helmut Graeb for making this possible.

Send an e-mail to henkel@kit.edu for any questions, ideas or inspirations of future *IEEE Design&Test* content you may have. Enjoy reading this issue! ■

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