A Complete Model of E^2PROM Memory Cells for Circuit Simulations

Paolo Pavan, *Member, IEEE*, Luca Larcher, *Member, IEEE*, Massimiliano Cuozzo, Paola Zuliani, and Antonino Conte, *Member, IEEE*

***Abstract*—E^2PROM memory devices are widely used in embedded applications. For an efficient design flow, a correct modeling of these memory cells in every operation condition becomes more and more important, especially due to power consumption limitations. Although E^2PROM cells are being used for a long time, very few compact models have been developed. Here, we present a complete compact model based on an original procedure to calculate the floating gate potential in dc conditions, without the need of any capacitive coupling coefficient. This model is designed as a modular structure, so to simplify program/erase and reliability simulations. Program/erase and leakage currents are included by means of simple voltage-controlled current sources implementing their analytical expression. It can be used to simulate memory cells both during read operation (dc conditions) and during program and erase (transient conditions) giving always very accurate results. We will show also that, provided good descriptions of degradation mechanisms, the same model can be used also for reliability simulations, predicting charge loss due to tunnel oxide degradation.**

***Index Terms*—Circuit simulation, computer aided design (CAD), integrated circuits, modeling, semiconductor memories.**

I. Introduction

In THE semiconductor industry, "modeling" and "characterization" have different meanings. Compact model means an analytic model of the electrical behavior of a circuit element, as used in a SPICE-like circuit simulator, and characterization means the procedure by which the parameters of a compact model are determined for devices in a particular integrated circuit (IC) manufacturing technology.

Compact models should be formulated physically, as functions of both the fundamental process parameters that control device electrical behavior and geometric layout parameters associated with a device (both adjustable layout parameters, such as device length and width and technology-dependent layout parameters derived from design rules, such as spacing between active areas and implant areas, etc.). There are three main reasons for preferring physically based compact models [1]. First, they provide the best basis for statistical modeling [2]. Second, they provide the best basis for mismatch modeling. Third, during the life cycle of a manufacturing technology there are changes, both in process flow and in design rules, that require to quickly retarget the design library.

Although the importance of E^2PROM memory cells has grown, very few compact models have been developed to be used in SPICE-like simulators [3] to study dc and transient behavior of complex circuits containing E^2PROM cells. E^2PROM cells are based on floating gate (FG) devices, which are metal-oxide-semiconductor (MOS) transistors where a conductive layer is interleaved between gate and channel and it is surrounded by insulator. The conductive layer is called FG. These devices' threshold voltage can be changed by injecting and/or extracting charge in/from the FG. Because of the lack of reliable compact models, in the industry complex circuits are usually simulated replacing FG memory devices with MOS transistors, whose threshold voltage is "manually" changed to simulate the erased and programmed states of the memory cell.

Different from compact models proposed in the past [3], [4], the complete compact model of E^2PROM cell we have developed is based on an original method to calculate FG potential in dc conditions [5]. This method does not use the fixed capacitive coupling coefficients any more and it is based on the solution of the charge balance equation at the FG node (which improves the FG voltage estimate, i.e., the overall modeling of the memory device) and on charge equations of the MOS transistor. Moreover, the compact model is designed to be modular, i.e., any transient phenomena (program, erase, leakage) can be included by adding a voltage controlled current source connected between FG and drain terminal. The transient simulation starts calculating the dc operating point using the FG voltage source (V_{FG}). Then, the FG voltage source is not used anymore, but the V_{FG} value used in transient simulations to bias the voltage controlled current sources connected to the FG is directly calculated by the SPICE-like circuit simulator adopted, which is able to solve the capacitive net in transient conditions.

Section II describes the basics of the model and Section III illustrates model parameters and their extraction procedure. Section IV deals with simulation of a single device: the dc behavior of an E^2PROM cell during read operation (Section IV-A) and the ability to simulate program and erase operations (Section IV-B). Section V describes how to use the model in the circuit simulation of E^2PROM memory products. Section VI will show possible uses of this model in reliability simulations and predictions. Conclusions follow in Section VII.

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P. Pavan is with Dipartimento di Ingegneria dell'Informazione, Università di Modena e Reggio Emilia, 41100 Modena, Italy (e-mail: paolo. pavan@unimore.it).

L. Larcher is with Dipartimento di Scienze e Metodi dell'Ingegneria, Università di Modena e Reggio Emilia, 42100 Reggio Emilia, Italy (e-mail: larcher.luca@unimore.it).

M. Cuozzo and P. Zuliani are with Central R&D, ST-Microelectronics, 20041 Agrate Brianza, MI, Italy (e-mail: massimiliano.cuozzo@st.com; paola.zuliani@st.com).

A. Conte is with the MPG, ST-Microelectronics, 95121 Catania, Italy (e-mail: antonino.conte@st.com).

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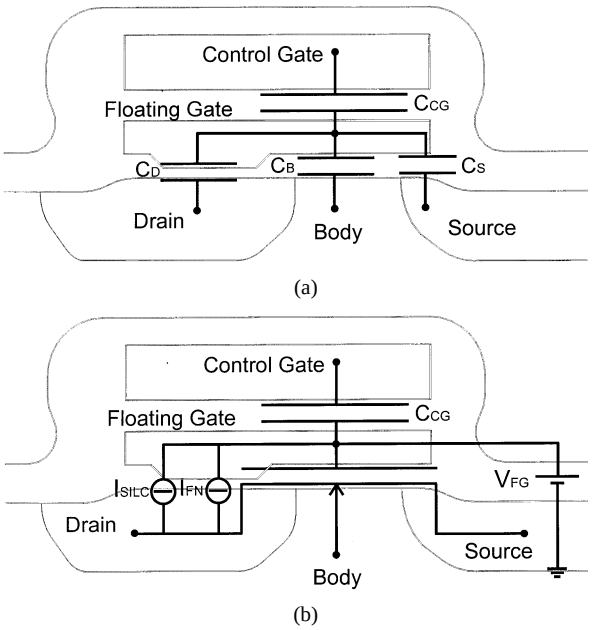


Fig. 1. (a). Traditional lumped element equivalent model of an E^2PROM memory cell, where C_D, C_S, C_B, and C_{CG} are the capacitances between FG and drain, source, body and CG, respectively. (b) Proposed complete model of the E^2PROM memory cell, which is comprised of: the C_{CG} capacitor; the MOS transistor equivalent to the E^2PROM cell with FG and CG short-circuited; the voltage-controlled voltage source, V_{FG}, between FG and ground; the P/E (I_{FN}) and leakage (I_{SILC}) current generators, that are activated during transient and reliability simulations.

II. FG Device Compact Model

The FG compact models in the literature are generally based on the "classic" lumped element description of the FG cell shown in Fig. 1(a), where also a schematic cross section of a generic FG device is shown. The basic concepts and the functionality of a FG device are easily understood if it is possible to determine the FG potential V_{FG} which is required for the correct modeling of memory operations. These "classic" models calculate it through capacitive coupling coefficients [$\alpha_j = C_j/C_{TOT}$; where j = S, D, B, CG, and $C_{TOT} = C_S + C_D + C_B + C_{CG}$, see Fig. 1(a)] [6] according to the following equation:

$$V_{FG} = \alpha_{CG}V_{CG} + \alpha_D V_D + \alpha_S V_S + \alpha_B V_B + \frac{Q_{FG}}{C_{TOT}} \quad (1)$$

where Q_{FG} is the charge stored in the FG.

However, these coefficients are not easy to measure, as the FG node cannot be directly accessed. Moreover, they depend on the applied terminal voltages [7], [8] and therefore, by considering them constant, as usually done, one introduces not negligible errors in V_{FG} calculation.

The model of E^2PROM memory cell we developed [5] has been implemented in a SPICE-like circuit simulator (ELDO [9]). It is composed by five circuit elements [see Fig. 1(b)]:

1) MOS transistor whose source (S), body (B), and drain (D) are S, B, and D, of the cell, and gate (G) is the FG of the cell;
2) capacitor connected between FG and control gate (CG) of the cell, C_{CG};
3) voltage-controlled voltage source, V_{FG}, between FG and ground;
4) voltage-controlled current source, I_{FN}, between FG and D, which models Fowler–Nordheim (FN) program and erase (P/E) currents;
5) voltage-controlled current source, I_{SILC}, between FG and D, which models stress-induced leakage currents (SILC), flowing across the tunnel oxide after P/E stresses.

The MOS transistor model can be one of the compact models implemented in the circuit simulator adopted (in our case, Philips MM9, but also BSIM3v3 and EKV models can be used). Thus, this FG device model takes advantage of the many efforts to improve and scale the MOS compact models.

The modular approach followed to develop this E^2PROM model allows to include in or remove from the basic structure different circuit elements to account for different phenomena into device simulations. For example: if E^2PROM reliability is not an issue, I_{SILC} current source can be removed or disconnected.

The voltage-controlled voltage source V_{FG} initializes the FG node to its correct value and it is needed to overcome the problem of simulating a capacitive net in dc conditions. This last circuit element is original and it contains the C code implementing the FG voltage calculation procedure, which is the core of this model and is based on the solution of charge balance equation at the FG node [5].

The voltage-controlled current source I_{FN} is necessary to simulate E^2PROM memory write operations. It models the FN current flowing across the tunnel oxide by means of its well-known analytical expression [10].

$$J_{FN}(F_{OX}) = A_{FN}F_{OX}^2 \exp\left(-\frac{B_{FN}}{F_{OX}}\right). \quad (2)$$

The exponential FN coefficient (B_{FN}) has been calculated according to its theoretical formula, assuming a poly Si/SiO_2 barrier height of 2.93 eV [11]. The pre-exponential FN coefficient (A_{FN}) has been derived from FN currents measured on MOS capacitors having oxide thickness and poly and substrate doping profiles equal to E^2PROM cell. The FN current is scalable by definition: A_{FN} is the area factor and the major dependence is on oxide field (F_{OX}), which depends on tunnel oxide thickness. Therefore, to correctly evaluate the oxide field, both charge quantization and poly depletion effects have been taken into account, since they increase both poly-Si/SiO_2 and Si/SiO_2 surface potential drops, thus significantly reducing the oxide field compared to that classically calculated. For this reason, the self-consistent model reported in [12] has been adopted. The oxide field calculated in this way has been fitted by an empirical formula and then inserted in the model. Following this approach, we can achieve very accurate oxide field calculations without the drawback of the large computation time required by the rigorous theoretical model.

It is worth noting that the proposed simulation methodology improves significantly the accuracy of the I_{FN} estimate. Particularly, both the new V_{FG} calculation procedure and the accurate oxide field calculation contribute to improve the accuracy of the model in transient conditions and extend the validity of the model to future scaled generations.

Moreover, it is worth pointing out that the F_{OX} calculation is consistent with FG charge variations at each time step Q_{FG}

which are induced by the tunnel current flowing either into (erase) or from (program) the FG node. In fact, the charge present on the FG node is always fully consistent with the FG potential, V_{FG}, thus enabling very accurate simulations of the E^2PROM cell program/erase transients.

The I_{SILC} voltage-controlled current source implements the analytical expression of the steady-state SILC first proposed in [19]. This empirical law describes SILC using a Fowler–Nordheim-like expression, where the exponential factor is calculated assuming a reduced oxide barrier height ($\Phi \approx 0.8$–1 eV) and the pre-exponential factor depends on the E^2PROM memory program and erased biases and number of P/E cycles undergone by the memory [17].

III. Model Parameters and Their Extraction Procedure

The methodology followed to extract model parameters can be divided into two subsequent parts.

The first part deals with the extraction of the dc parameters of the MOS transistor in Fig. 1(b). This MOS transistor is the "dummy cell," that is the E^2PROM cell where FG and CG are short-circuited. The usual MOS extraction strategy can be used with reasonable results paying attention to the slightly different physics of the dummy cell. In fact, the narrow and short geometry, the lack of lightly doped drain, and pocket implant determine a less ideal behavior such as larger drain-induced barrier lowering effect and higher multiplication current.

The second part deals with the extraction of the overlap capacitance values. These parameters can be evaluated from capacitance–voltage (CV) measurements performed on a dummy cell array. In order to separate the drain and source overlap capacitance contribution from the channel one, it is necessary to perform a CV measurement in accumulation condition separating the source and drain current from the bulk. From the accumulation branch of such CV measurement it is possible to calculate the drain-FG overlap capacitance, C_D. It is important to pay attention to the parasitic interconnect capacitance contribution that could affect the measurement. In this case, it would be better to use a dedicated layout to minimize such contribution. By repeating the measurement for the source terminal of the array, also the source-FG overlap capacitance, C_S, can be retrieved. The bulk-FG coupling capacitance can be evaluated as well by analyzing in this case the inversion branch of the CV curve.

Additional parameters are: 1) CG to FG capacitance C_{CG}; 2) tunnel region area A_{TUN} that can be directly calculated from the layout of the cell; and 3) tunnel oxide thickness $T_{OX,T}$ which is given by process.

IV. Single-Cell Simulations

A. DC (Read Operation)

The model proposed in this paper allows an accurate reproduction the dc behavior of E^2PROM memory cells manufactured in an existing technology (0.35 μm). Examples of fitting capabilities of our model are shown compared to experimental data for E^2PROM cells with $W = 0.3\ \mu m$, $L = 0.75\ \mu m$ and $C_{GC} = 3$ fF [see Fig. 2(a)–(c)]. As shown in the figures, the agreement between current–voltage (*I–V*) measurements and simulations is excellent without the need of any free parameter to adjust fitting quality. As the E^2PROM memory cell is constituted by the FG device in series with the select transistor, this last one has also to be taken into account to simulate correctly the behavior of the actual memory cell. This can be done in two different ways: 1) the select transistor model card is directly included and the Spice-like model of the memory cell is constituted by the series of the select transistor and FG transistor. 2) Since the gate bias of the select transistor is as high as to deliver the BL bias to the cell drain without significant losses (when the memory cell is addressed), the select transistor can be simply modeled by a small resistance connected in series with the drain of the "dummy" transistor. Therefore, the

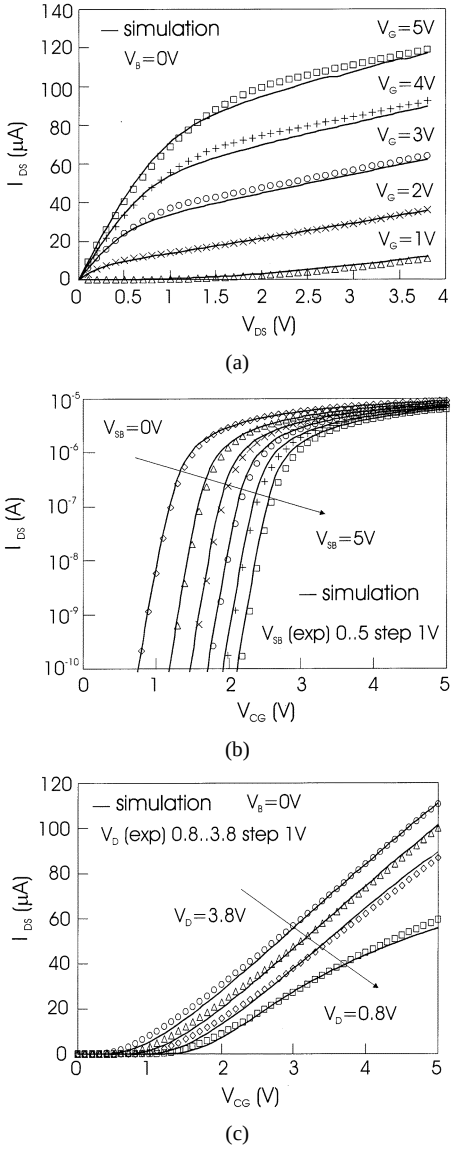


Fig. 2. Comparison between experimental curves (symbols) and simulations (solid lines) obtained by our model by assuming the FG residual charge $Q_{FG} = -0.65$ fC are shown for a E^2PROM cell ($W = 0.3\ \mu m$, $L = 0.75\ \mu m$ and $C_{GC} = 3$ fF). (a) Output characteristics $I_{DS} - V_{DS}$ ($V_B = 0\,V$, $V_{CG} = 1, 2, 3, 4$, and 5 V). (b) Transcharacteristics $I_{DS} - V_{CG}$ ($V_{DS} = 0.1\,V$, $V_{SB} = 0, 1, 2, 3, 4$, and 5 V). (c) Subthreshold transcharacteristics $I_{DS} - V_{CG}$ ($V_B = 0\,V$, $V_{DS} = 0.8$, 1.8, 2.8, and 3.8 V).

contribution of the select transistor can be effectively accounted for by slightly increasing the drain resistance of the "dummy" transistor. Conveniently, this can be done automatically by applying the MOS parameter extraction procedure to the series of the dummy cell and the select transistor.

Results obtained in the two cases are very similar (data in Figs. 2(a)–(c) refer to the second solution), therefore, the second approach has been preferred as it requires only the extraction of one model-card ("dummy" cell). Note that the E^2PROM bias sets shown in Figs. 2(a)–(c) are used only in the characterization activity of these memory devices, being different in the final E^2PROM memory product. Moreover, this model correctly describes the W and L dependence of V_T of the cell [5]. In fact, the effects of geometry dependences are included in the MOS compact model used for the dummy cell.

B. Transient (Program and Erase Operations)

The analysis of program/erase transients of E^2PROM memory cells has been tackled in the literature either by implementing new experimental methods [13], or (mostly) by developing models able to simulate current and threshold voltage characteristic during write transients [14], [15]. Typically, threshold voltage V_T is measured during write and it is used to derive the tunnel current since $I_T = C_{CG} dV_T/dt$.

To erase the E^2PROM memory cell considered in this study, a voltage ramp is applied to the CG, while S, D, and B are pinned to ground. The program operation is performed applying the voltage ramp to the D, whereas B and CG are grounded and S is left floating. In both cases, a Fowler-Nordheim current flows across the tunnel oxide.

Fig. 3(a) and (b) shows V_T variations for different ramp rise times both during program and erase. Fig. 4(a) and (b) shows the I_T current that can be simulated and derived in the same conditions. As shown, the agreement is again excellent. To be really accurate, though, some discrepancy in the tunnel current simulations can be observed. Precisely, I_T derived from measured data does not reach the same peak value predicted by the model and also it does not flatten in the peak region.

In Fig. 5(a), we measured with an oscilloscope the real voltage ramp applied to the CG (solid line) and we noticed that it is quite different from the nominal one (dashed line). This significantly affects both V_T and I_T curves. Both threshold voltages and tunnel currents simulated applying the real voltage ramp agree remarkably with measurements, whereas if we use the nominal voltage ramp we cannot simulate correctly the experimental data; see again Fig. 5(b). This indeed confirms the high accuracy of this model, but at the same time it opens the discussion on the usual methods used to analyze program/erase current in E^2PROM memory cells.

The "real" shape of the CG voltage pulse has a strong impact on V_T and I_T. We have separately considered the effects of three parameters which can be used to describe the real voltage pulse: ΔV, T1, and T2, [see the inset of Fig. 5(a)]. Among them, only the maximum difference between the nominal ramp and the real ramp, ΔV, has a significant influence on both threshold voltage and tunnel currents. Particularly, it influences I_T in two ways [see Fig. 5(b)]: on increasing ΔV we observe 1) the max-

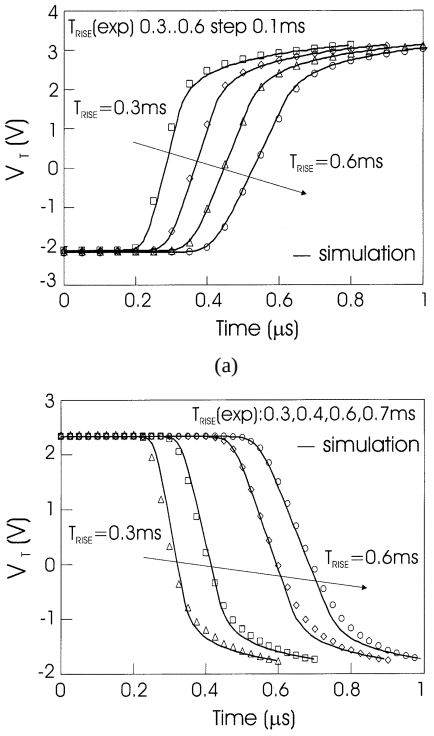


Fig. 3. Experimental (symbols) and simulation (solid lines) results of (a) ERASE and (b) PROGRAM operations performed on the same E^2PROM cell ($W = 0.3\ \mu m$, $L = 0.75\ \mu m$, and $C_{GC} = 3$ fF). ERASE bias conditions: V_{CG} is ramped from 0 to 12 V with different T_{RISE}, while D, S, and B are grounded. PROGRAM bias conditions: V_D is ramped from 0 to 12 V with different T_{RISE}, while CG and B are grounded and S is left floating. The threshold voltage V_T is measured as the CG voltage at which $I_D = 4\ \mu A$, when $V_{DS} = 0.8$ V.

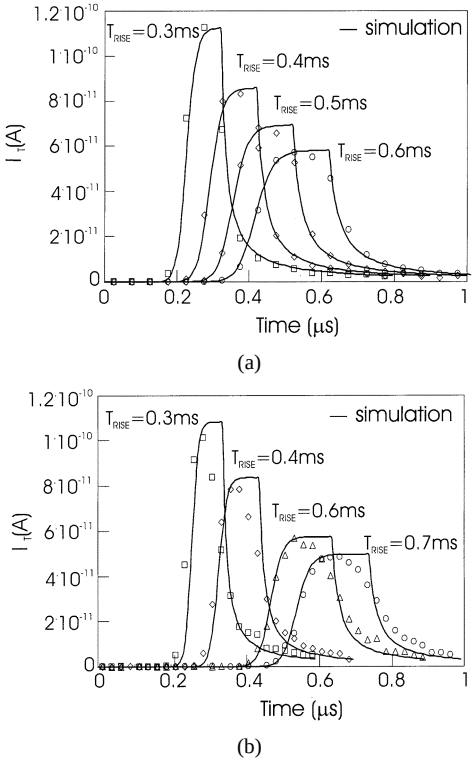


Fig. 4. Experimental (symbols) and simulation (solid lines) results of tunnel current derived in the same conditions as in Fig. 3(a) and (b).

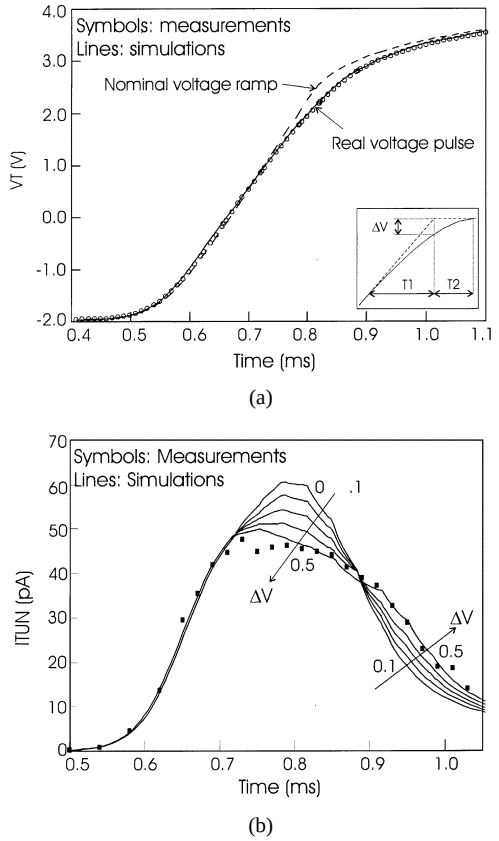


Fig. 5. (a). Comparison between measured and simulated threshold voltage of an E^2PROM ($W = 0.3\ \mu m$, $L = 0.75\ \mu m$, and $C_{GC} = 3$ fF) memory cell applying both the nominal and the real voltage erase pulse on the CG. In the inset, nominal and real voltage pulses applied to the CG of the cell are depicted. (b) Tunnel current simulated for different values of ΔV are shown (lines) and compared with measurement (symbols).

imum value of tunnel current reduces significantly (17% reduction when $\Delta V = 0.5$ V) and 2) the "time window," defined as the time interval for which $I_T > 20$ pA, increases (15% increase when $\Delta V = 0.5$ V). Since T1 and T2 have a negligible influence on V_T and I_T, the effect of a real voltage pulse can be completely characterized only by ΔV, which can be calibrated to fit the measured I_T (both current peak and "time window"). To ease this calibration, we derived a simple empirical rule: a 10 μs increase in the measured "time window," compared to that simulated with the nominal voltage pulse, translates to a 0.1-V increase in ΔV, for this E^2PROM technology.

V. Circuit Simulations

The E^2PROM circuit we have investigated comes from a Smart Card application. For this reason, the sensing scheme that has been developed [16] is accurate in terms of current detection, it ensures large sensitivity in differentiating programmed and erased states and at the same time it is fast enough to work with the microcontroller clock speed. The sensing scheme is also reliable in terms of disturbs and cycling.

Fig. 6(a) shows a block representation of the read path. The sensing scheme generates the voltages to bias the bit lines (BL) and CG of the cells in the array. BL voltage should be large to drive enough current in the cell but also small to avoid any stress effect during read. CG voltage (V_{CG}) is generated to bias

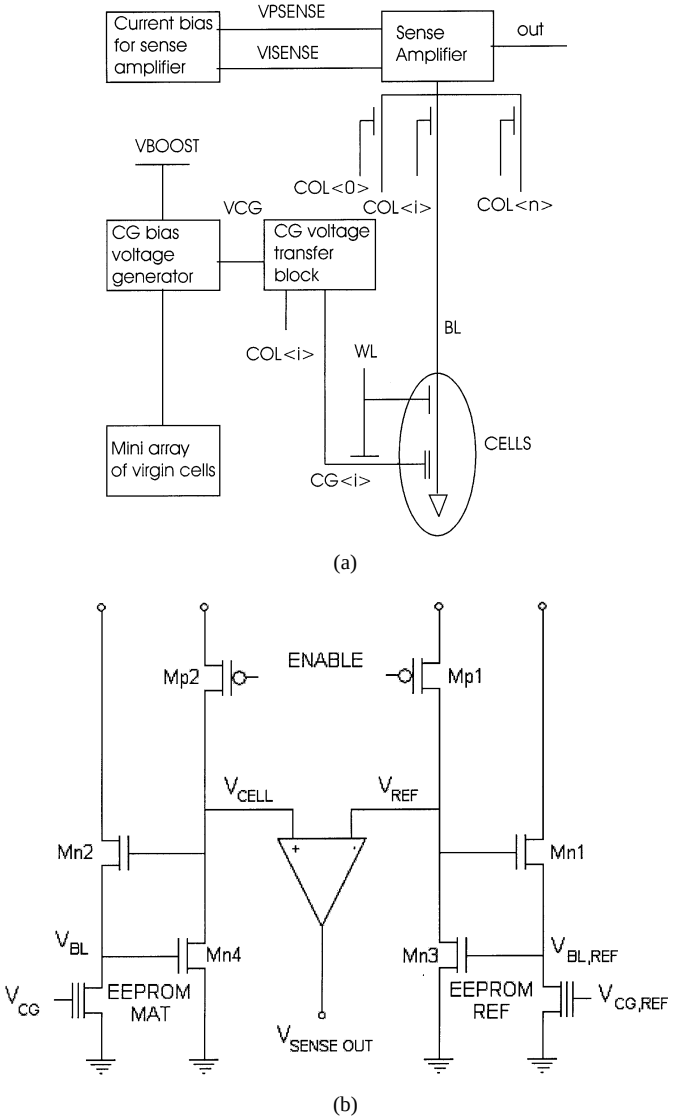
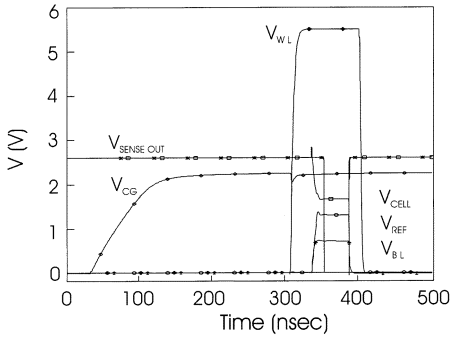


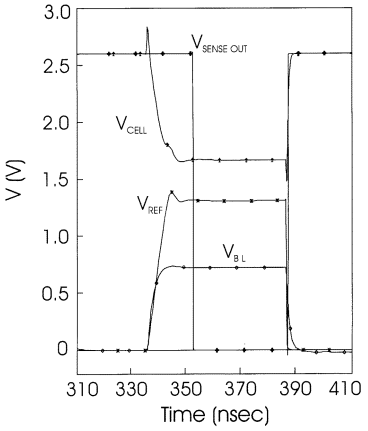
Fig. 6. (a) Block diagram of the read-path circuits implemented in [16] and used for simulations. (b) Schematic of the sense amplifier and the direct *I–V* conversion circuits of the E^2PROM memory considered, used for circuit simulation.

a virgin cell to have a current level between erased and programmed states. V_{CG} is dynamically applied to the CG only during read, to eliminate any unwanted disturb. A virgin cell is, therefore, used to generate the CG voltage and, therefore, a compact model is needed to perform correct simulations. Usually, MOS transistors whose threshold voltage is "manually" changed to account for the programed/erase memory cell were included in circuit simulations to simulate E^2PROM memory cells. In this way, the actual memory cell influence is not simulated and approximate results are obtained. Instead, this new model allows correct simulations of any circuit that includes a memory cell: read paths, nonvolatile latches, X and Y decoders, and voltage pumps.

The schematic of the sense amplifier circuit simulated is shown in Fig. 6(b). It is a classic scheme where active load p-channel transistors are biased to provide the wanted constant current, thus allowing a controlled trip point voltage and temperature compensation. Trip point means voltage level of



(a)



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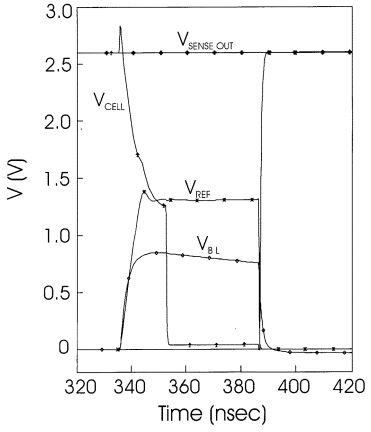

(c)

Fig. 7. Control signals and sense amplifier output obtained from read-path circuit simulations in the two cases of a programed (a)–(b) and erased (c) E^2PROM cell.

the BL during reading. The structure is fully differential to have a good noise immunity. Mn1 and Mn3 and Mn2 and Mn4 provide the *I–V* conversion to bias the reference cell and the cell to be read in the matrix. V_{CELL} and V_{REF} are compared to generate the V_{SENSE_OUT} digital level.

We have checked the major differences obtained by using this new model instead of an nMOS transistor. We did not observe major differences in waveforms of read path circuit signals. As shown in Fig. 7(a)–(c), we can simulate (a) control signals and the output of the sense amplifier either with a (b) programmed cell or (c) an erased cell.

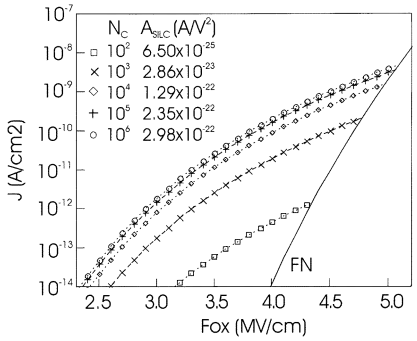

Fig. 8. SILC current for different number of cycles N_C. The corresponding values assumed for A_{SILC} are also reported.

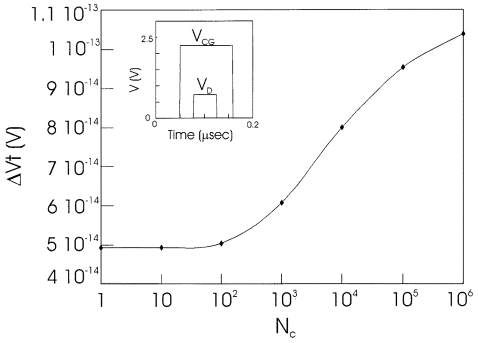

Fig. 9. V_T shift induced by a single read operation on increasing the P/E cycles on the E^2PROM cell considered. Read conditions are: $V_{CG} = 2.5$ V and $V_D = 0.8$ V, as shown in the inset.

A 7%–10% smaller energy given by a V_{BOOST} generator is simulated using the new model, due to the correct description of capacitances and loads.

VI. Reliability Simulations

This compact model can be also used to simulate reliability effects in E^2PROM cells [17]. An additional voltage-controlled voltage source is added to the standard configuration of the model to implement an analytical expression of SILC current. To this purpose, we adopted the empirical law proposed in [18] and [19], which describes SILC by using an FN-like expression, with a reduced oxide barrier height and a pre-exponential factor, A_{SILC}, which is proportional to the current density and the amount of charge injected during stress [17].

To relate SILC effects to E^2PROM reliability, A_{SILC} has been expressed as a function of the P/E cycle number, N_C, calculating the write current density and the average charge exchanged during P/E operations from write simulations in standard conditions. The resulting SILC curves are plotted for different N_C values in Fig. 8: SILC current increases on increasing the number of P/E cycles.

With this upgraded model, we simulated SILC-related effects: read-disturbs and retention. Simulations show that the read operation does not affect the threshold voltage of programed/erased cells, since both the oxide field and the time involved are too low to induce any FG charge variations, regardless the SILC magnitude. As shown in Fig. 9, the threshold voltage shift, ΔV_T, induced by a read cycle is insignificant for cycled E^2PROM cells. In fact, we simulated that the number

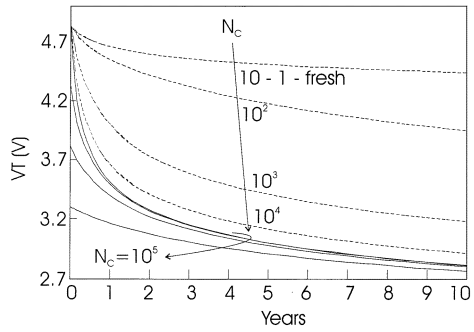

Fig. 10. Threshold voltage during storage at room temperature of the $\mathrm{E^2PROM}$ cell. Devices after 10^5 cycles have been simulated with different starting $\mathrm{V_T}$ values.

of read cycles required to have a half a volt $\mathrm{V_T}$ shift is around $5 \cdot 10^{12}$ also for the most damaged cell ($\mathrm{N_C} = 10^6$), thus demonstrating that SILC affects negligibly $\mathrm{V_T}$ during the read of the cell and, therefore, is not a concern for $\mathrm{E^2PROM}$ data storage.

On the contrary, retention losses appear to be strongly related to SILC magnitude. To this regard, Fig. 10 shows simulations of retention experiments: the threshold voltage shifts occurring in an erased $\mathrm{E^2PROM}$ cell which is left unbiased for ten years at room temperature.

We have considered only erased $\mathrm{E^2PROM}$ cells, since reliability issues are more critical in this case due to the larger storage oxide field (compared to that of a programed cell).

In $\mathrm{E^2PROM}$ cells after 10^5 cycles, we have also simulated threshold voltage shift occurring when initial $\mathrm{V_T}$ values much larger than the standard ones (for which, memory retention requirements are guaranteed) are used to accelerate retention experiments. To this regard, Fig. 10 shows that: 1) as largely expected, the threshold voltage shift after ten years is proportional to the number of P/E cycles of the cell, $\mathrm{N_C}$, since SILC rises on increasing $\mathrm{N_C}$. Note that all curves overlap for $\mathrm{N_C} \leq 10$, since in these conditions the FN current contribution is dominant (see Fig. 8). 2) If we use a large initial $\mathrm{V_T}$, the final threshold voltage does not depend on it, i.e., on the storage field. In fact, curves for $\mathrm{N_C} = 10^5$ and different initial $\mathrm{V_T}$ converge to a similar value after four years, thus underlining the importance of a correct experimental evaluation of retention, since a large $\mathrm{V_T}$ value to accelerate retention extrapolation gives origin to a transient decrease that converges to the "long term" decay curve, which depends only on the oxide degradation level, that is proportional to $\mathrm{N_C}$.

VII. Conclusion

We have presented a complete compact model for $\mathrm{E^2PROM}$ cells. This model does not use capacitive coupling coefficients and it is based on charge balance equation at the FG node. It is easily scalable and is very simple to implement, since its parameters can be determined using standard extraction procedures. Its accuracy is great because it depends on that of compact MOS models adopted and its computation time is comparable to that of a simple MOS transistor.

By adding some appropriate voltage/controlled current source, we were able to describe correctly transient behaviors during program and erase operations. This model can be easily included in circuit simulators and it does not increase simulation time. If degradation mechanisms can be described analytically, they can be included and thus reliability simulations and predictions are also possible.

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Paolo Pavan (M'94) received the electrical engineering degree (on latch-up and hot-electron degradation phenomena in MOS devices) and the Ph.D. degree (on impact ionization phenomena in advanced bipolar transistor) from the University of Padova, Padova, Italy, in 1990 and 1994.

From 1992 to 1994, he was with the University of California, Berkeley, where he studied radiation effects on MOS devices and circuits. Recently, his interest focused on the characterization and modeling of Flash memory cells and on the development of new nonvolatile cells. He authored and coauthored technical papers, invited papers, and two chapters in books. Since 1994, he has been with the University of Modena and Reggio Emilia, Reggio Emilia, Italy, where he is currently an Associate Professor of Electronics.

Luca Larcher (M'98) received the electronic engineering degree (where he researched the modeling of gate oxide currents in MOS devices) and the Ph.D. degree (on the compact modeling of nonvolatile [E^2PROM and Flash) memories] from the University of Padova, Padova, Italy, in 1998 and 2002.

He is currently a Researcher of Electronics with the University of Modena and Reggio Emilia, Reggio Emilia, Italy. His research interests include the reliability and the compact modeling of MOS and Floating Gate memories. In this field, he focused on the modeling of stress and radiation induced leakage currents, channel-hot electron currents and MOS gate capacitance. He has authored and coauthored technical papers.

Massimiliano Cuozzo was born in Rome, Italy, in 1971. He received the physics degree from the University of Rome "Tor Vergata," Rome, in 1995 and the Ph.D. degree from the University of Napoli, Naples, Italy, in 1999.

Since 2000, he has been a Compact Modeling Engineer with the Non Volatile Process Development Group, ST-Microelectronics Central R/D, Agrate Brianza, Italy. He authored and co-authored technical papers. His research interests cover both process technology and modeling aspects.

Paola Zuliani, photograph and biography not available at the time of publication.

Antonino Conte (M'97) was born in Agrigento, Italy, in 1966. He received the electronics engineering degree (*cum laude*) from the University of Palermo, Palermo, Italy, in 1992.

After two years in Siemens Tlc, Cassina de Pecchi, Milan, Italy, he joined ST-Microelectronics, Catania, Italy, and in 1996, he became Designer in Non-Volatile Memory for Smart Card applications. Currently, he is responsible for the NVM macrocell design development team. His fields of interest are EEPROM and Flash memory macrocells for very low-voltage application. He holds ten patents and has authored technical papers.