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Electronic transport mechanisms in scaled gate-all-around silicon nanowire transistor arrays

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Low-frequency noise is used to study the electronic transport in arrays of 14 nm gate length vertical silicon nanowire devices. We demonstrate that, even at such scaling, the electrostatic control of the gate-all-around is sufficient in the sub-threshold voltage region to confine charges in the heart of the wire, and the extremely low noise level is comparable to that of high quality epitaxial layers. Although contact noise can already be a source of poor transistor operation above threshold voltage for few nanowires, nanowire parallelization drastically reduces its impact.
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Further reduction in the size of the metal-oxide semiconductor field-effect transistors (MOSFETs) used in computer chips will require more complex geometries to enhance the gate control of the current flow in the transistor channel.[1] Gate-all-around (GAA) is the optimum device configuration to electrostatically control a transistor with narrowest channel length[2] and minimize the leakage current when the device is in the off-state, making the device operate with less dissipation per switching event. Several GAA geometries are possible and have been demonstrated either in horizontal[3] or vertical configuration.[4–7] Although technical solutions are envisioned to ultimately scale the gate length L_g of transistors down to few nanometers,[5] many open questions remain on the impact of the transition from 1D (either long gate or large width) to transistors scaled in all dimensions on device operation. Among them, the quality of devices fabricated and sources of fluctuation that could induce poor transistor operation or dispersion in electrical properties should be addressed clearly to propose solutions for ultimate integration. However, classical characterization techniques, such as mobility extraction, are insufficient to provide information on the devices quality at ultimate scaling, because the mobility can collapse at such small gate lengths.[8–11] Low-frequency noise can be a very precise technique for characterizing electronic transport in low-noise nanodevices.[12,13] Previous studies of low-frequency noise in transistors with a nanowire (NW) channel have addressed the potential of this architecture for extremely low noise level. However, they have either been performed with very long channel[14–17] or on short channel,[12,18] but in a specific configuration, not acceptable for large-scale integration.

Figure 1(a) shows a schematic view of the device,[5] which is a scaled version of a p-type (doping level 8×10^{18} cm^{-3}) junctionless transistors.[19] Figure 1(b) shows a cross-sectional transmission electron microscopy image of the final device, which integrated massively parallel, dense NW arrays with symmetrically silicided Source/Drain and scaled metallic gate-all-around ($L_g \sim 14$ nm) architectures. As expected from a top-down patterning of single-crystal silicon coupled with sacrificial thermal oxidation, NWs obtained are of high crystalline quality with an atomic-level-smooth Si-SiO_2 interface[35] (see Fig. 1(c)). Fig. 1(d) offers a schematic view of the device illustrating the different sources of noise. It includes noise at contacts, mobility fluctuation due to defects in the crystal, and single-charge trapping-detrapping at gate oxide interface. This schematic view concerns any scaled GAA transistor.

Figure 2 shows the low-frequency noise-normalized spectra (S_I/I^2) of a single NW (Fig. 2(a)) and an array of 2916 NWs (Fig. 2(b)), at gate voltages (V_G) of 0 V and −0.5 V. In both cases, the threshold voltage was estimated to be ∼−0.4 V, in agreement with Ref. 5. The spectra followed an $1/f$ dependence, except for the single scaled NW, for which a slope of $1/f^2$ was observed at gate voltages above the threshold voltage. The $1/f^2$ slope, observed after a corner frequency of a Lorentzian spectrum, is typical of a dominant active defect in low-dimensional transistors.[20] Because the time constant associated with the defect may vary between wires, the $1/f$ noise was observed for the array of wires as an integration of many Lorentzian spectra.[21] We discuss the microscopic origin of the defect below.

Figures 3(a) and 3(b) show the full gate-voltage dependence from subthreshold to linear region of the normalized power spectrum current noise S_I/I^2 at 10 Hz for a single NW and an array of scaled NW devices. The curve shapes exhibited two regimes, similar to Schottky barrier nanoscale field-effect transistors (FETs).[22] For such transistors, the noise equation considers the contribution of the channel and the contacts

$$\frac{S_I}{I^2} = (1-\eta)^2 \frac{S_{Ichannel}}{I^2} + \eta^2 A \left(\frac{q}{kT}\right)^2 \frac{1}{\left(1 - e^{-q\eta\frac{V_d}{kT}}\right)^2} \frac{1}{f}, \quad (1)$$

where A (in V^2) is a parameter for noise-amplitude comparison, $\eta = R_C/(R_C + R_{Ch})$, with contact and channel resistances R_C and R_{Ch}, respectively, and f is the frequency. The first and second terms are related to the channel and contact

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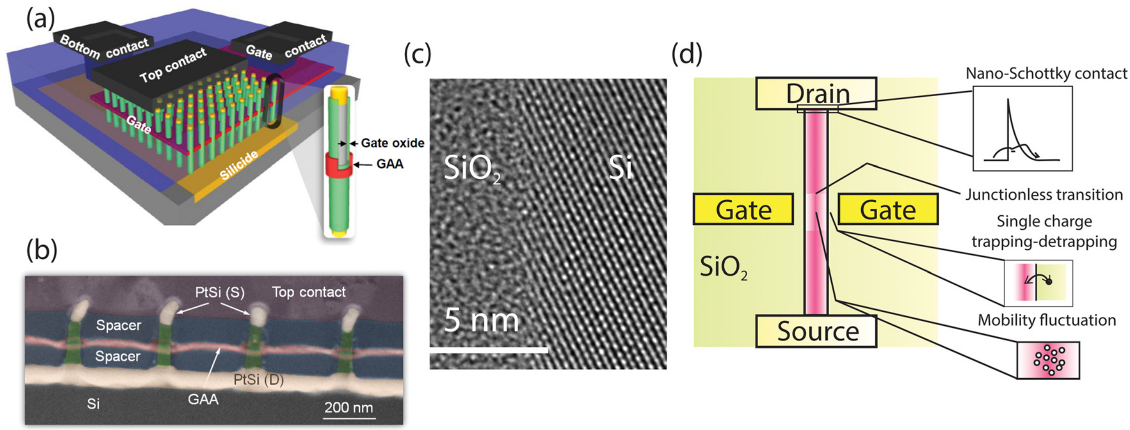

FIG. 1. (a) Representation of a vertical NW array-based FET. Schematic view of a vertical FET device implemented on a dense NW array, with extrinsic access connecting different levels (top, bottom, and gate contacts). Inset: Zoom of a NW in cross-sectional view in the top part shows the gate stack, composed of the gate oxide and the metal gate surrounding the NW. Each termination is silicided symmetrically with respect to the gate. (b) Transmission electron microscopy image of the vertical NW array transistor, in tilted view with false color, showing a gate surrounding each NW, symmetrical silicided S/D (PtSi) contacts and 60-nm low k dielectric spacers separating the S/D contacts to the gate. (c) TEM image: Zoomed image showing Si-SiO2 interface. Vertical axis corresponds to the (100) crystal axis. (d) Schematic view of the device, showing the different noise sources that are likely in this device, including contact noise, mobility fluctuation in the channel, and single-charge trapping/detrapping at the gate oxide interface. Panels (a) and (b) are reprinted with permission from G. Larrieu and X.-L. Han, Nanoscale 5, 2437 (2013). Copyright 2013 RSC publishing group -Reproduced by permission of The Royal Society of Chemistry (RSC) [http://pubs.rsc.org/en/content/articlelanding/2013/NR/c3nr33738c#!divAbstract].[5]

noises, respectively. In the subthreshold regime, the first term dominates, particularly when the channel resistance is large (we can consider $\eta \sim 0$ at $V_G \sim 0$ V). As a consequence, we first analyse results below threshold voltage to get information on the charge transport in the wire and gate-oxide interface and then address the contact noise level by analyzing results above threshold voltage.

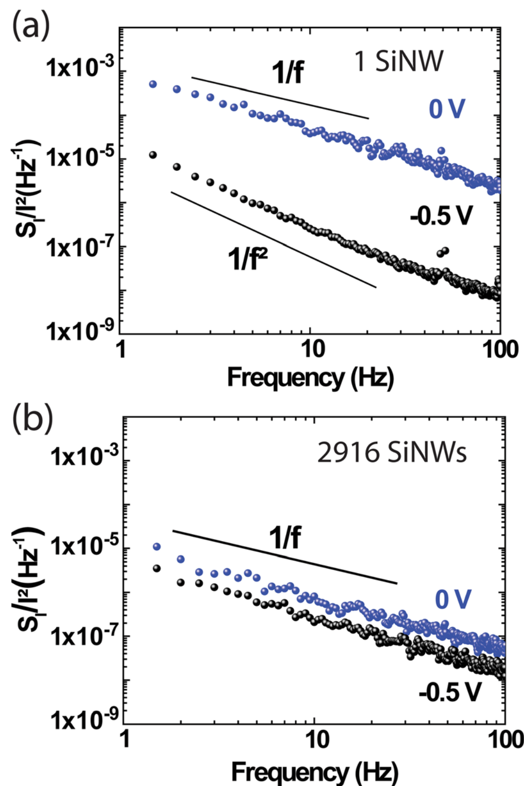

FIG. 2. Normalized power spectrum noise as a function of frequency at $V_G = 0$ V (blue curve) and -0.5 V (black curve) for 1 (a) and 2916 scaled SiNWs (b).

Below threshold voltage, if we suppose that the trapping/detrapping noise at the channel/oxide interface is dominant, we can derive the following equation for a gate-all-around transistor, starting from number fluctuation theory:[23,24]

$$\frac{S_I}{I^2} = \left(\frac{\ln 10}{S}\right)^2 \frac{q^2 N_{ot}.2\pi r L}{N C_g{}^2} \frac{1}{f}, \tag{2}$$

where S is the subthreshold swing; N_{ot} is the density of the oxide traps; $C_g = 13.8$ aF is the gate capacitance for a single NW, estimated from the cylindrical capacitor approximation; $r = 15$ nm is the NW radius; and N is the number of nanotransistors in parallel. Using (2), we obtained $N_{ot} = 1.6 \times 10^8\,\text{cm}^{-2}$ for a single transistor ($S \sim 200$ mV/dec) and $N_{ot} = 5.4 \times 10^{10}\,\text{cm}^{-2}$ for 2916 nanotransistors ($S \sim 85$ mV/dec). Consideration of short channel effect in Eq. (2) would not have much affected results, because we do not observe a serious degradation of S in our device. Such values are typical for low-noise p-type transistors.[24] This finding highlights that the use of sophisticated vertical transistor technology does not increase the density of the oxide traps.

Considering a surface of $1.4 \times 10^{-11}\,\text{cm}^2$ per transistor, we obtained an average of less than one trap per transistor. This observation led us to ask where the noise originated from in a transistor without an oxide trap, such as the transistor with $N = 1$ ($N_{ot} = 1.6 \times 10^8\,\text{cm}^{-2}$ corresponds to 0.003 traps). Furthermore, the random telegraph signal (RTS) (i.e., the two-level current fluctuation due to single charge trapping/detrapping) was not observed in the subthreshold region. Thus, in this regime, due to the small density of active traps, mobility noise[25] was likely the dominant source of noise.[26] Hooge's empirical formula[25] for mobility fluctuation in Metal-Oxide-Semiconductor FETs is still valid for scaled FETs

$$\frac{S_I}{I^2} = \frac{\alpha_H q \mu V_D}{I L^2 f}, \tag{3}$$

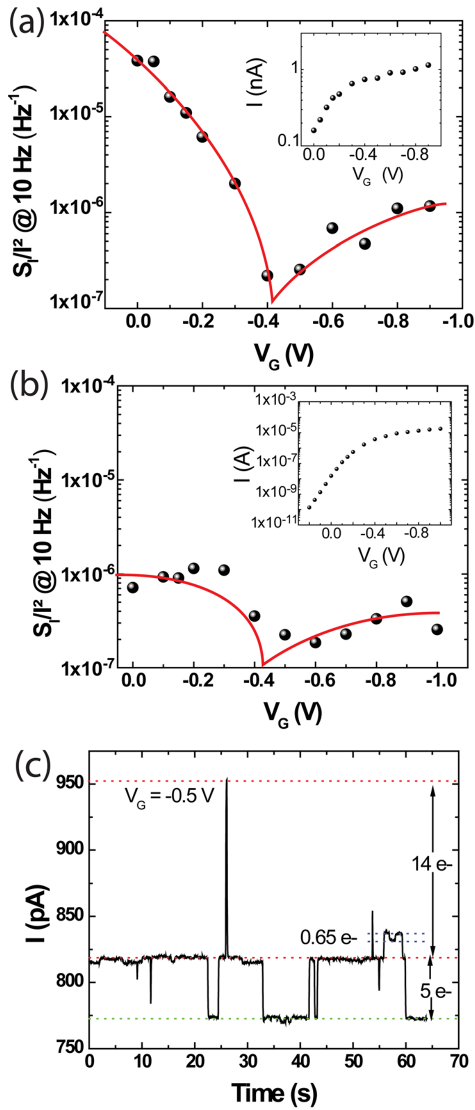

FIG. 3. Normalized power spectrum noise as a function of gate voltage for 1 (a) and 2916 (b) scaled SiNWs. Red lines are guides. Respective I-V_G curves for both graphs are shown in the inset. (c) Time-dependent drain current at $V_G = -0.5$ V. Discrete fluctuations of drain current ΔI are correlated to an equivalent charge q^* at the channel/gate-oxide interface using $q^* = \Delta I\, C_G/g_m$. Values > 1 suggest that such discrete fluctuation steps are related to fluctuations at the nano-Schottky contact.

where α_H is the Hooge's constant, μ is the mobility, and $V_D = 50$ mV is the drain voltage. We obtained $10^{-5} < \alpha_H < 5 \times 10^{-5}$ for 1 or 2916 scaled NWs at $1 < \mu < 5\,\text{cm}^2/\text{V s}$. In high-quality material, such as epitaxial layers, α_H values range from 10^{-6} to 10^{-4}.[26] Consequently, the mobility degradation observed in these devices was unlikely to be related to low crystal quality (Fig. 1(c)) or poor oxide interfaces. This small Hooge's constant is the smallest ever reported for scaled nanowire transistors. For example $\alpha_H \sim 4.2 \times 10^{-3}$ was found for a GAA (35 nm gate length) transistor with a III-V NW.[27] For gate lengths below 15 nm, we can not compare our results since there was no report of Hooge's constant at such scaling. In the subthreshold region, we can reasonably consider that mobility fluctuation was the dominant source of noise. More importantly, the observed absence of RTS and low noise amplitude indicated a "volume" conduction. Although such transport in the heart of the wire has already been suggested for long NWs[15,17] with junctionless architecture or due to quantum confinement effect (our argument based on RTS is only meaningful for scaled devices), it was not ensured that such behavior would have been observed for GAA transistors with $L_g < 15$ nm. This clearly indicates the potential of such GAA technology for future scaling.

Above the threshold voltage, we expected that carriers would be accumulated at the NW interface under a strong electric field, but also that the contact would play a larger role in charge transport (reduced channel resistance). The contact noise can be measured,[22,28,29] even when the contact resistance is not dominant compared to channel resistance.[22] We confirmed that contact noise was observed in these scaled NWs by carefully analyzing the discrete drain current steps ΔI in the time domain (Fig. 3(c)) at $V_G = -0.5$ V. The equivalent charge fluctuation Δq at the gate oxide interface was estimated by $\Delta q = (\Delta I/g_m)\, C_g$, where $g_m = (\partial I/\partial V_G)$ is the transconductance.

We identified three different step amplitudes, corresponding to 0.65, 5, and 14 elementary charges q (Fig. 3(c)). Only values $\leq q$, due to image charge effects,[12] could be obtained by trapping/detrapping noise at the channel/oxide interface. Values $> q$ could be explained by trap-induced tunneling at Schottky contacts.[22] The quantitative extraction of N_{ot} above the subthreshold regime was not possible with this technique, because noise was dominated by charge fluctuations at the contacts. However, the background noise for a single NW was well below a single charge trapping/detrapping at the oxide interface (Fig. 1(d)), indicating that N_{ot} was low in the few worst-case traps per wire. Using Eq. (1), we quantitatively estimated the normalized noise above the threshold voltage from the drain voltage dependence,[22] obtaining $\eta = 0.03$ and $A = 10^{-6}$ for 1 NW. These values show that these nanoscale contacts are of low noise amplitude since A (when normalized by contact area) is two orders of magnitude lower than that found for a conventional transistor with p-type segregated Schottky barrier.[22] The finding of $\eta = 0.03$ indicated that the contact resistance was only 3% of the overall resistance, but still in the tens of kΩ per contact, several times larger than that found for a carbon nanotube transistor.[30]

Figures 4(a) and 4(b) show the normalized noise at 0 V (subthreshold) and -0.8 V (linear regime) for scaled NWs with N varying between 1 and 2916. On average, S_I/I^2 scaled as $1/N$ in both cases, is in agreement with (1) if we consider that A scales as the contact surface.[22] However, the dispersion was very large for noise above the threshold voltage and at small N. This large dispersion arose from the random number of traps at the contacts and the high variability of the impact of each trap on noise amplitude (ΔI varied between 0.1 and 14 q: Fig. 3(d)), due to the exponential dependence of the fluctuation at Schottky contacts[22] or trap-assisted tunneling.[31–33] For the array of 3 × 3 NWs, the random telegraph signal amplitude is as large as 25% of the current level (see Fig. 4(b), inset), in the limit of acceptable noise level for transistor operation in logic circuits.[34] Noise dispersion from wire to wire was expected to follow a log-normal distribution, according to binomial law, $\Delta\log[(S_I/I^2)]_N = \Delta\log[(S_I/I^2)]_1/N^{1/2}$ (see fits with dashed red lines in Fig. 4). Thus, use of an array of NWs increased the

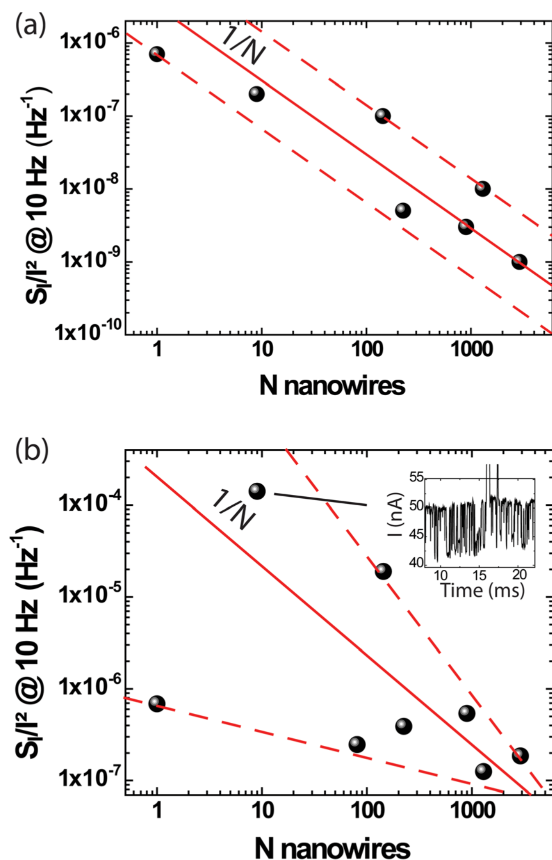

FIG. 4. Normalized power spectrum current noise as a function of N at $V_G = 0$ V (a) and -0.8 V (b). Dashed lines are fits to the fluctuation of normalized noise amplitude. Inset: Drain current fluctuation as a function of time for a 3 × 3 NW array at $V_G = -0.6$ V.

current level, reduced the variability in contact resistance[35] or threshold voltage,[5] but also reduced relative noise amplitude and dispersion. As a consequence, although contact noise can already be a limiting factor for correct transistor operation at 14 nm gate length when it is composed of few wires (Fig. 4(b), inset), NW parallelization drastically reduces its effect, which ensures reliability for the overall device.

The role of contacts in ultra-scaled devices has already been addressed for nanowires, carbon nanotube,[30] or graphene[36] transistors through series resistance. However, we have shown that the main problem at ultimate scaling may come from contact noise that can induce fluctuations in the same range as the drain current. This observation is surely not limited to our architecture. Interestingly, theoretical equation of low-frequency noise derived for ballistic transistors has also a similar shape as (1), with contact noise dominant contribution at high V_G.[29] In Ref. 19, fluctuation in the range of 25% of drain current is seen for a carbon nanotube transistor with $L_g = 9$ nm, but has not been discussed. In addition, since dispersion of this fluctuation from device to device was not addressed, it is probably not the upper limit. The important general result demonstrated here for nanocontacts is that contact induced drain current fluctuation is drastically reduced by parallel operation of scaled nanotransistors. Using Eq. (1), this contact noise would still be sustainable for few nm gate lengths with 40 NWs.

Our results also suggest that the reduced mobility is intrinsic to ultimately scaled devices in general (gate length $\ll$ 100 nm), as was previously reported for transistors with more conventional architectures based on experimental[37] and modeling[38] studies. A recent theoretical study predicts that such limit may not be observed in graphene.[39] To date, theoretical studies on nanowires have mainly focused on mobility estimation for other aspects, such as the NW diameter with infinitely long wires[40] or the impact of the surface roughness.[41] The GAA architecture, thanks to its axial symmetry, is a perfect test-bed for theoretical investigation of scaling on electronic transport mechanism and comparison with experimental data. Understanding the origin of reduced mobility with scaling will soon become a crucial issue for the future of silicon as the dominant material in processors. The architecture presented here could be extended to III-V NWs. These NWs are promising materials for transistor arrays due to their large intrinsic mobility although there is, to date, no report confirming that mobility will not collapse with a scaled configuration. Reports of noise at the single-NW level have indicated that the mobility noise[27] ($\alpha_H \sim 4.2 \times 10^{-3}$) and oxide trap density[42] ($N_{ot} \sim 2.5 \times 10^{12}\,\mathrm{cm}^{-2}$) are not optimized yet. Carbon nanotube GAA FETs, due to their ballistic behavior at $L_g < 50$ nm, could be immunized to mobility decrease at short gate length, but not to contact noise.

Ultimate scaling is not only of interest for processors applications. Scaled Ion-sensitive Field-Effect transistors (ISFETs) have already shown a great potential for electrochemical sensing applications.[43] The array of scaled transistors that show ultra-low noise in the subthreshold region could be operated as very efficient sensors with a nanofluidic liquid gate, instead of Cr gate. Since voltage noise scales also as $1/N$, such sensors could reach a voltage noise level of 3.10^{-5} $V/Hz^{1/2}$ @ 10 Hz with 2916 NW, which corresponds to an accuracy of 0.05% of a typical Nernstian pH shift in 1 Hz bandwidth.

In conclusion, we presented insights into the electronic transport mechanism of the scaled Gate-all-around SiNW array transistor by using low-frequency noise analysis. Interestingly, quantitative estimation of mobility noise is still valid and the extracted small Hooge's constant is a signature of volume conduction within a high-quality Si crystal. Above the threshold voltage, the large RTS amplitude in single or few NWs could be attributed to charge fluctuations at the contact interface. This contact noise reaches already the limit of correct transistor operation for the noisiest 14 nm-gate length transistors with few NWs but our study indicates that parallelization of gate-all-around transistors is an efficient way to reduce this contact noise. This result is surely not limited to the sole SiNW transistors with GAA architecture. We suggest that dispersion and fluctuation of electrical characteristics should be addressed clearly for all technologies. Our results indicate that whereas transistors with few nm gate lengths should be operational with GAA architecture, technological breakthrough for contacts, theoretical modeling for scaled FETs, and choice of channel material will surely become the roadmap of research on nanodevices in the near future.

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