Short Papers

Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method

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***Abstract*—A new low-cost test method for analog integrated circuits, called the oscillation test, is presented. During the test mode, the circuit under test (CUT) is converted to a circuit that oscillates. Faults in the CUT which deviate the oscillation frequency from its tolerance band can be detected. Using this test method, no test vector is required to be applied. Therefore, the test vector generation problem is eliminated, and the test time is very small because only a single output frequency is evaluated for each CUT. The oscillation frequency may be considered as a digital signal and therefore can be evaluated using pure digital circuitry. These characteristics imply that the oscillation-test strategy is very attractive for wafer-probe testing as well as final production testing. In this note, the validity of the proposed test method has been verified throughout various examples such as operational amplifiers, amplifiers, filters, and analog-to-digital converters (ADC's). The simulations and practical implementation results affirm that the presented method assures a high fault coverage.**

I. Introduction

Due to the new development of integrated circuit technology and the market potentials, the trend of designing mixed-signal ASIC's has increased. Analog testing is a challenging task, and is considered as one of the most important problems in analog and mixed-signal ASIC design. The specifications of analog circuits are usually very broad, which result in long testing time, poor fault coverage, and the requirement of a dedicated test equipment.

Testing analog circuits can be accomplished using functional testing [1]–[4], dc testing [5], [6], power-supply quiescent current ($I_{\rm DDQ}$) monitoring [7], [8], and digital signal processing (DSP) techniques. Various designs for testability (DFT) rules have been used in conjunction with the mentioned test methods. These techniques are employed during the design stage to increase the controllability and observability and to ease the test problem.

The effectiveness of the above methods depends on the selection of suitable test vectors. When the complexity of the circuit under test (CUT) increases, the problem of generating optimal test vectors assuring high fault coverage becomes critical. Furthermore, the process of choosing a suitable form of excitation signals and results evaluation is time consuming. Built-in self-test structures based on the above test methods require the use of specialized input stimulus generation and output evaluation hardware which introduce a significant area overhead. The majority of applications require a stimulus generator which guarantees very good accuracy and/or supports a wide range of frequencies.

In an attempt to overcome some of the above-mentioned limitations, we develop a new test method for analog circuits which does not require the test vector generation and application procedure. As a digital output test strategy, it can be simply integrated with test methods dedicated to the digital part of the chip. The aim of this note is to present and justify our general idea. The note is organized as follows. Section II is dedicated to presenting the proposed test method. Then, in the Section III, the presented test strategy is applied to some analog and mixed-signal circuits. Fault coverage of the presented method is discussed in Section IV.

Manuscript received February 22, 1996; revised July 5, 1997. This paper was recommended by Associate Editor S. Reddy.

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Publisher Item Identifier S 0278-0070(97)07564-7.

II. Oscillation Test Strategy

In this note, we present a new test method for analog and mixed-signal circuits based on transforming the CUT to an oscillator [9], [10]. Using this method, the complex analog circuit is partitioned into functional building blocks such as amplifier, operational amplifier (OA), comparator, Schmitt trigger, filter, voltage reference, oscillator, phase-lock loop (PLL), etc., or a combination of these blocks. During the test mode, each building block is converted to a circuit that oscillates. The oscillation frequency $f_{\rm OSC}$ of each building block can be expressed as a function of its components or performances. The building blocks that generate inherently a frequency, such as oscillators, do not need to be rearranged, and their output frequency is directly evaluated.

The oscillation-test method allows removing the analog test vector generator and output evaluators, and consequently reduces the test complexity, area overhead, and test cost. As no test vector is required in this test strategy, testing of high-frequency analog circuits becomes easier. The test time is small because only a frequency per building block must be verified. Fig. 1 illustrates the application of the proposed test method as a DFT technique to improve the testability and ease the test problem. All operations are managed using the control logic (CL). In the test mode, the CUT is divided into building blocks that are converted to oscillators using some additional circuitry. An analog multiplexer (AMUX) selects the output of the converted building block, and its oscillation frequency can be externally evaluated using test equipment. Before starting the test procedure, the functionality of the test structure is verified by activating the *STest* signal.

We define the observability of a fault in a component C_i as the sensitivity of the oscillation frequency $f_{\rm OSC}$ with respect to the variations of the component C_i. To increase the observability of a defect in a component, the sensitivity of the oscillation frequency with respect to that component should be increased. In other words, during the conversion process of the CUT to an oscillator, the oscillator architecture must be chosen to ensure the maximum possible of the CUT components' contribution in determining the oscillation frequency. Existing faults in the CUT related to components that are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the deviation of the oscillation frequency from its tolerance band may be employed to detect fault.

The tolerance band of $f_{\rm OSC}$ for each CUT is determined using a Monte Carlo simulation, taking into account the nominal tolerance of all important technology and design parameters. The Monte Carlo analysis also evaluates the stability of the CUT in the test mode. The oscillator should be stable in all iterations of the Monte Carlo simulation. The accuracy necessary for additional circuitry should be about the same accuracy provided for other CUT components.

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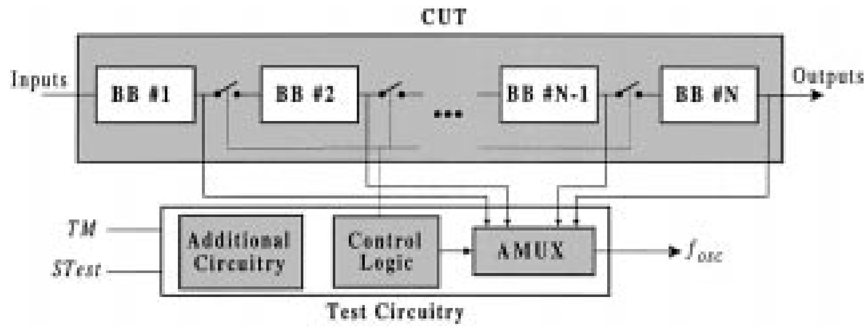

Fig. 1. Simplified test structure of the oscillation-test strategy (BB: building block, TM. test mode, *STest:* self-test mode, AMUX: analog multiplexer).

TABLE I
CLASSIFICATION OF OCCURRENCE PROBABILITY OF FAULTS IN A CMOS TECHNOLOGY [15]

Fault class	Device failures	Interconnect defect
More probable	Gate-drain short Gate-source short	Short between diffusion lines
Probable	Open on drain contact Open on Source contact	Aluminum polysilicon cross-over broken
Less probable	Gate-substrate short Open on gate contact	Short between Aluminum lines

III. CASE STUDIES AND RESULTS

To be able to evaluate the proposed test method, we first define our fault modeling for analog circuits. Then, some analog and mixed-signal building blocks are used as test vehicles to examine the efficiency of the test method, but the method is not constrained to these examples in its application.

A. Analog Fault Modeling

In order to verify the fault coverage of the presented test method, an accurate and realistic fault list is required. A fault can be either parametric (soft) or catastrophic (hard). Parametric faults, caused by statistical fluctuations in the manufacturing process, comprise the small deviation of CUT parameters from their tolerance band. Catastrophic faults are introduced by random defects, and result in failures in various components. They are provoked, for example, by dust particles on a photolithographic mask, and cause either short and open circuits or a large deviation of CUT parameters from their tolerance band such as the width-to-length (W/L) ratio of a MOS transistor [11], [12].

Many studies have been devoted to determining the dominant fault types and to defining the appropriate fault models. Research results denote that 80–90% of observed analog faults were catastrophic faults consisting of shorts and opens in diodes, transistors, resistors, and capacitances [13], [14]. It was also noted that a test method which detects 100% of catastrophic faults also found the majority of soft faults depending on the deviation value of the soft fault [12]. The occurrence probability of faults has been also considered [15] as presented in Table I. As a conclusion, the studies indicate that catastrophic faults, and especially short faults, are dominant in both bipolar and CMOS processing technologies. Therefore, a comprehensive list of catastrophic faults is inducted and simulated for all case studies. A set of parametric faults is also injected depending on the type of the CUT.

The catastrophic faults considered in this study comprise all possible shorts between circuit nodes and open faults at all circuit nodes excluding the transistor gates. An open fault is simulated by introducing a 10 M-Ω resistor. A short fault is modeled by a 10 Ω resistor.

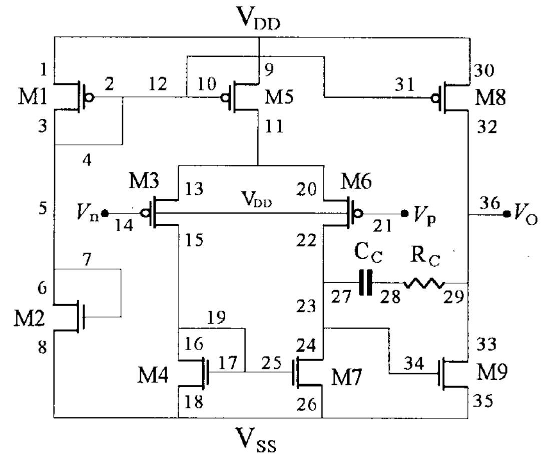

Fig. 2. Compensated CMOS operational amplifier.

B. Operational Amplifier (OA) Testing

OA is the most frequently encountered block in analog and mixed-signal circuits. For analog functional blocks with embedded OA's, the test procedure will be easier and a higher fault coverage may be obtained if the OA's are tested before. Therefore, the importance of developing an efficient technique to test OA is obvious.

Fig. 2 shows the schematic representation of a two-stage CMOS OA that is considered as the CUT. Before presenting the test technique, important characteristics of the OA will be summarized.

The total amplifier dc open-loop gain is given by

$$a_V = \frac{g_{m3}g_{m9}}{(g_{ds6}+g_{ds7})(g_{ds8}+g_{ds9})} \tag{1}$$

where the channel conductances g_m and g_{ds} are defined as

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{I_D} \cong \sqrt{(2\mu_O C_{\rm OX} W/L)|I_D|} \tag{2}$$

$$g_{ds} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{I_D} \cong I_D\lambda \tag{3}$$

in which μ_O is the channel surface mobility, $C_{\rm OX}$ is the capacitance per unit area of the gate oxide, W and L are the effective channel width and length, respectively, and λ is the channel length modulation parameter of the transistor. I_D represents the quiescent current, and is provided by $M1, M2,$ and $M5$ transistors.

The unity-gain bandwidth of the OA is calculated as follows:

$$\omega_T = 2\pi f_T = a_V p_1 \tag{4}$$

TABLE II
IMPORTANT CHARACTERISTICS OF THE OA

Parameter	Simulation Results
Unity-gain bandwidth (f_T)	26 MHz
Gain at dc (a_V)	91.6 dB
Phase margin (φ_M)	84°
Slew rate (SR)	> 110 V/µs
Offset voltage (V_{OS})	5 µV

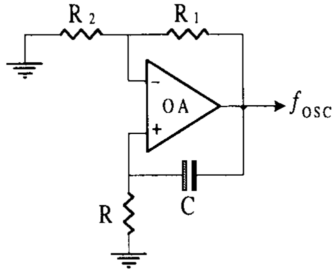

Fig. 3. Single-OA sinusoidal oscillator.

in which p_1 represents its dominant pole. As the OA is compensated, its transfer function can be approximated to a single-pole transfer function given by

$$a_V(s) = \frac{a_V}{1 - s/p_1}. \tag{5}$$

Table II summarizes the important characteristics of the OA under test. These results have been obtained with a 5 pF capacitor load.

One of the most effective techniques of converting an analog building block to an oscillator consists of adding a feedback loop to its structure, and then adjusting the feedback elements to establish and sustain oscillations. Depending on the CUT, the feedback loop can be negative, positive, or a combination of both.

In this example, both positive and negative feedback loops have been added. Fig. 3 shows the schematic view of this oscillator. The positive feedback loop consists of an RC delay, and the negative feedback comprises a voltage divider. To facilitate the mathematical analysis, the combination of feedback loops is presented by a single negative feedback block in which the positive feedback appears as a term with a negative sign. The feedback block converts the OA under test to a second-order system which has the potential of oscillation. The new transfer function is derived as follows:

$$A_V(s) = \frac{a_V(s)}{1 + a_V(s)f(s)} \tag{6}$$

where

$$f(s) = G - \left(\frac{-s/p_2}{1 - s/p_2}\right) \tag{7}$$

in which $G = R_2/(R_1 + R_2)$ and $p_2 = -1/RC$. Substituting $f(s)$ into $A_V(s)$, we obtain

$$A_V(s) = \frac{a_V p_1 (p_2 - s)}{s^2 + ((1-G)a_V p_1 - (p_1 + p_2))s + (G a_V p_1 p_2 + p_1 p_2)}. \tag{8}$$

The system poles are obtained by equating the denominator of the new transfer function to zero. In order to construct an oscillator from this new transfer function, its poles must be placed on the imaginary axis on the s domain by forcing the coefficient of the term s to zero, which is realized by proper selection of the value of G as follows:

$$G = 1 - \frac{p_1 + p_2}{a_V p_1}. \tag{9}$$

TABLE III
CMOS OA FAULTS WHICH MAINTAIN THE OSCILLATIONS

Fault	Voltage Level (V)	Oscillation Frequency Deviation
N9,11-S*	<-4.01 , 3.03>	+ 20%
N31,32-S*	<-2.47 , 2.8>	- 15%
N28,29-S*	<-4.53 , 4.76>	- 14%
N28-O*	<-4.63 , 4.72>	+ 85%
All Other Faults	**No Oscillation**	**No Oscillation**

N9,11-S: Short between nodes 9 and 11. N28-O: Open at node 28.
*: Representing a set of schematically redundant faults.

The natural oscillation frequency for the new system is given by

$$\omega_{\rm osc}^2 = G a_V p_1 p_2 + p_1 p_2 = a_V p_1 p_2 - p_2^2. \tag{10}$$

Assuming $RC = 10^{-7}$, we found $G = 0.94$ to establish sustained oscillations. The oscillation frequency $f_{\rm OSC}$, obtained by simulation, is approximately 6 MHz. The maximum achievable frequency using this oscillator can be calculated by equating to zero the derivative of $\omega_{\rm osc}$ with respect to p_2, which results in $p_2 = a_V p_1/2$ and $G \approx 0.5$. Therefore, $\max\{\omega_{\rm osc}\} = a_V p_1/2$ can be obtained by selecting $RC = 1.23 \times 10^{-8}$ and $R_1 = R_2$.

The oscillation frequency depends strongly on important characteristics of the OA under test which are determined by all components of the OA. Existing faults in the OA will deviate its characteristics from their nominal value, which can be monitored by observing the oscillation frequency. In order to evaluate the testability of the proposed test techniques, the process of introducing shorts and opens at devices is used with five faults per transistor [11]. Faults such as circuit node opens and shorts between different nodes of the CUT are also injected. Thirty-six different nodes are identified on the OA schematic. Note that some nodes that seem schematically redundant such as 8, 18, 26, and 35 are not physically redundant. The total number of 657 faults, consisting of 27 open faults and 630 short faults ($C_2^{36} = 36!/(2!(36-2)!)$, is used as the fault dictionary for the op-amp under test. In this particular case, the majority of injected faults resulted in a loss of oscillation. The remaining injected faults caused significant deviation of the oscillation frequency from its nominate value. Table III presents the results of the oscillation frequency for the faults which preserve the oscillations, but deviate the frequency from its nominal value. Faults which result in a loss of oscillation are not presented in this table. Only one fault of each schematically redundant fault set is presented in the table. As the results demonstrate, all injected faults have been manifested themselves by affecting the oscillation frequency, and therefore can be detected. Using a Monte Carlo analysis, the tolerance band of the oscillation frequency is determined to be [−5.5%, +4%].

C. Bipolar Amplifier Testing

An amplifier is designed to have a limited and precise gain with desired input and output impedance. Test approaches developed in the previous section, therefore, can be adapted to amplifiers. As the amplifier has a limited gain, the negative feedback is not necessary. In order to be able to practically verify the effectiveness of the introduced test method, a bipolar amplifier has been realized using discrete elements. Then the amplifier has been incorporated in an oscillator, a comprehensive list of possible catastrophic and parametric faults has been injected, and their effect on the oscillation frequency $f_{\rm OSC}$ has been observed. The discrete amplifier is shown in Fig. 4. It consists of three stages: a differential amplifier to provide gain, a level shifter to cancel the dc component, and an emitter follower to guarantee low output impedance. General-purpose

TABLE IV
INJECTED FAULTS IN THE BIPOLAR AMPLIFIER WHICH RESULT IN A DEVIATION OF THE OSCILLATION FREQUENCY FROM ITS NOMINAL VALUE; FAULTS CAUSING THE LOSS OF OSCILLATIONS AND REDUNDANT FAULTS ARE NOT PRESENTED

Fault	Output Voltage Level (V)	Oscillation Frequency Deviation	Fault	Output Voltage Level (V)	Oscillation Frequency Deviation
N1-O	<2 , -2.2>	+ 14 %	R_2 (50%↑)	<-0.5 , 1.6>	+ 9 %
N17-O	<-1 , -5.5>	- 29 %	R_5 (50%↓)	<3 , 8>	+ 54 %
N28-O	<-1.4 , 1.5>	+ 73 %	R_5 (50%↑)	<-12.5 , -9>	- 60 %
N18,19-S*	<-4.48 , 4.65>	- 20 %	R_6 (50%↓)	<-1.85 , 2.4>	- 53 %
N22,23-S*	<11 , 13>	+ 32 %	R_6 (50%↑)	<-2 , 2.1>	- 27 %
R_1 (50%↓)	<-0.4 , 1.7>	+ 10 %	R_7 (50%↓)	<-1.8 , 1.9>	- 22 %
R_1 (50%↑)	<-6.4 , 2.4>	- 18 %	R_7 (50%↑)	<-2.8 , 2.8>	- 27 %
R_2 (50%↓)	<-6.2 , 2.4>	- 14 %			

N1-O: Open at node 1, N18,19-S: Short between nodes 18 and 19, *: Representing a set of schematically redundant faults.

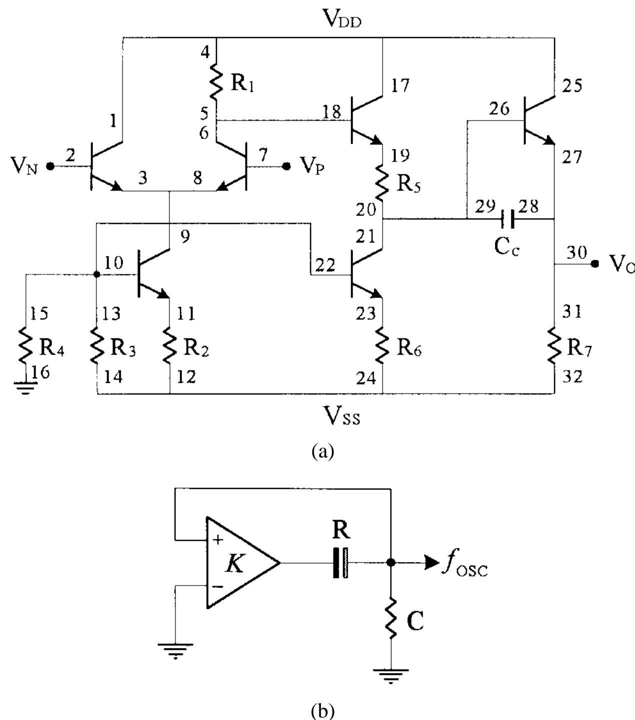

Fig. 4. Schematic representation of (a) the discrete bipolar amplifier, and (b) the technique to convert it to an oscillator. $R_1 = 10\ \mathrm{k}\Omega$, $R_2 = 1.8\ \mathrm{k}\Omega$, $R_3 = 900\ \Omega$, $R_4 = 10\ \mathrm{k}\Omega$, $R_5 = 35.8\ \mathrm{k}\Omega$, $R_6 = 1.8\ \mathrm{k}\omega$, $R_7 = 4.7\ \mathrm{k}\Omega$, and $C_C = 1$ nF.

transistors (2N222) and 10% resistors were used. Prior to practical realization, the amplifier was simulated using Hspice. Resistor R_5 was chosen to be adjustable to cancel the offset voltage after realization. The final component values are given in Fig. 4. The low-frequency open-loop gain K and the cutoff frequency f_C of the amplifier are 29 and 180 kHz, respectively.

The technique employed in this section to rearrange CUT to an oscillator is first to convert it to a bandpass system having a greater than unity gain within its passing band, and then to establish a positive feedback by simply connecting the output to the input. As a result, the existing noise is bandpass filtered and amplified in the loop, and produces an oscillating signal. The amplitude of oscillations is limited by the nonlinear effects of the active amplifier. The oscillation frequency is determined by the bandwidth and the gain of the system. It is obvious that if the bandpass system is selective and tuned to a single central frequency, the oscillating signal will be a pure sinusoid equal to the central frequency.

Based on the above technique, the first step to construct the oscillator is to convert it to a bandpass system. As the amplifier is a low-pass system, by cascading a simple high-pass RC filter, it becomes a bandpass system which can be converted to an oscillator by feeding back its output to its input [Fig. 4(b)]. Practical implementation using $R = 350\ \Omega$ and $C = 1.5$ nF for the feedback resistor and capacitor resulted in an oscillation frequency of 78 kHz.

In order to determine the fault coverage the following faults have been practically injected: 1) open at all circuit nodes shown in Fig. 4, including opens at collector, base, and emitter of transistors; 2) short between collector and base, base and emitter, and collector and emitter of all transistors; and 3) 50% of deviation in resistor and capacitor values in both directions. The majority of injected faults resulted in the absence of oscillations. Faults which resulted in a deviation of the oscillation frequency are presented in Table IV. These results affirm that 100% of injected faults are detectable by the output frequency evaluation. Redundant faults and faults resulting in the loss of oscillations are not shown in the table.

D. Myoelectrical Signal Amplifier/Filter Testing

In this section, the oscillation-test method has been applied to test a practical circuit [17] to show how the test method is applied to more complicated circuits. The idea of generating more than one oscillation frequency per building block and optimizing the set of oscillation frequencies is demonstrated through this example. The CUT, illustrated in Fig. 5(a), is a simple amplifier and filter unit to interface myoelectrical signals coming from a patient to the computer [17]. Fig. 5(b) reveals the test solution for this circuit based on the method presented in this note. During the normal operation of the circuit, S_1 selects V_{IN}, S_2 selects the ground, S_3 is closed, S_4 is open, and S_5 is closed. Switches have been realized using a CMOS structure to minimize the undesired effects introduced due to their presence [18]. The CUT is simulated using Hspice without and in the presence of switches. The results, shown in Fig. 6, demonstrate no significant effect on the functionality of the CUT due to the existence of switches.

The technique employed in this section to convert the CUT to oscillators is to establish a positive feedback for a bandpass system that has a greater than unity gain in its passband. To increase the number of oscillation frequencies, the capacitor C, which is used to bypass the capacitor $C1$, has been added. As a result, six different oscillation frequencies can be produced using only two test points.

1) Switch S_1 selects the ground, S_2 selects the output of OA2, S_3 is closed, S_4 is open, and S_5 is closed. The oscillation frequency f_{OSC1} is observed at the output of OA2. All CUT components are involved in the test.

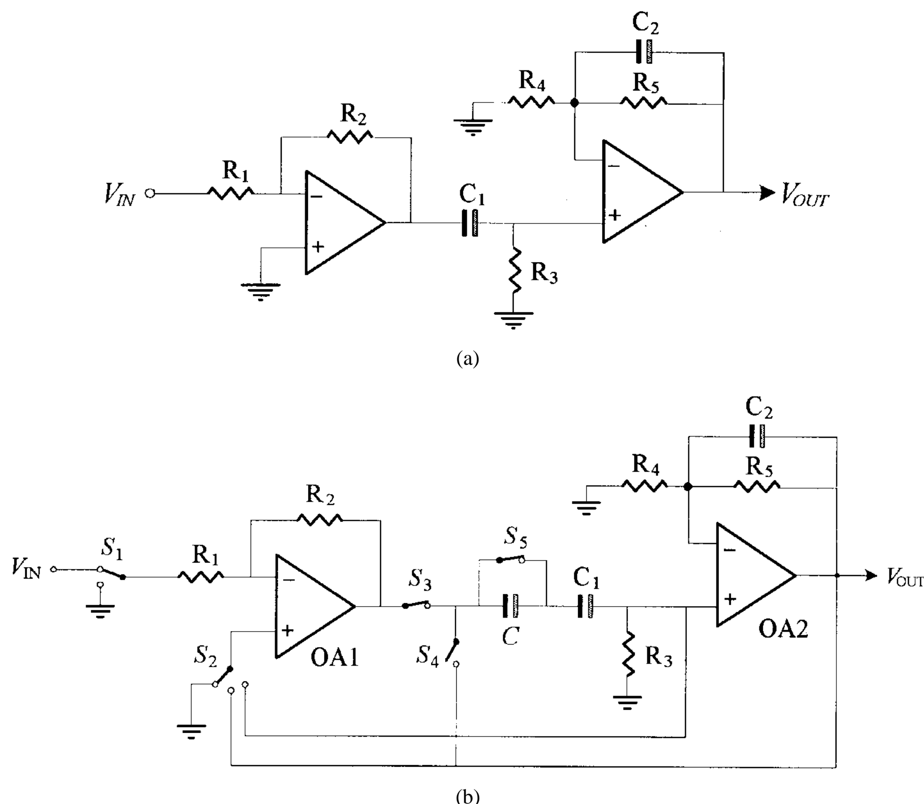

Fig. 5. (a) Practical myoelectrical signal amplification and filtering circuit and (b) its testable version based on oscillation-test method. $R_1 = 10c$ kΩ, $R_2 = 330$ kΩ, $R_3 = 1$ MΩ, $R_4 = 10$ kΩ, $R_5 = 330$ kΩ, $C_1 = 330$ nF, $C_2 = 4.7$ nF, and $C = 50$ pF.

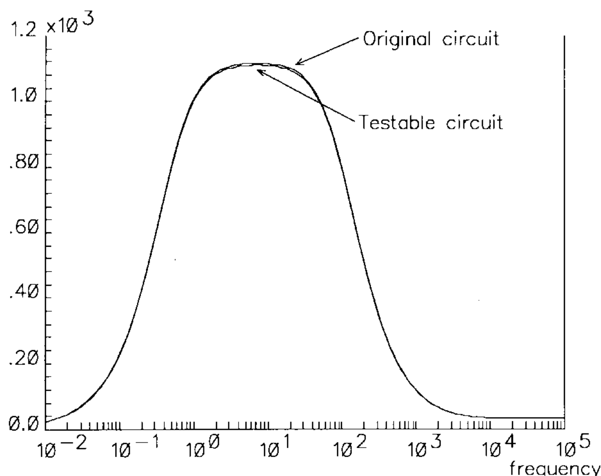

Fig. 6. Simulation result of ac characteristics of the myoelectrical signal processor.

2) The same as case 1), except that the switch S_5 is open. The output of OA2, f_{OSC2}, is used as the test point. All CUT components, except C_1, are implicated in the test.
3) Switch S_1 selects the ground, S_2 selects the positive input of OA2, S_3 is closed, S_4 is open, and S_5 is closed. The oscillation frequency f_{OSC3} is observed at the output of OA1. The involved components are R_1, R_2, R_3, C_1, and OA1.
4) The same as case 3), except that the switch S_5 is open. The oscillation frequency f_{OSC4} is observed at the output of OA1 to monitor the faults in R_1, R_2, R_3, and OA1.
5) Switches S_1 and S_2 select the ground, S_3 is open, S_4 is closed, and S_5 is closed. The oscillation frequency f_{OSC5} is observed at the output of OA2. The involved components are R_3, R_4, R_5, C_1, C_2, and OA2.
6) The same as case 5), except that the switch S_5 is open. The oscillation frequency f_{OSC6} is observed at the output of OA2 to detect the faults in R_1, R_2, R_3, and OA1.

It should be noted that there are many other possibilities to convert the CUT to oscillators with or without adding some additional circuitry. Generally, increasing the number of oscillators for a circuit under test improves the test precision.

The amplifier/filter, shown in Fig. 5(a), has been realized using μA 741 and discrete elements. Available CMOS analog switches, DGP201A from Siliconix Inc., have been used to convert the CUT to oscillators based on Fig. 5(a). All possible shorts and opens on resistors and capacitors have been injected. Furthermore, 20 and 50% of deviations from the nominal value in both directions have been introduced for all passive components. All catastrophic faults, except open at C_2, are detectable using only the first oscillator which produces f_{OSC1}. The fault at C_2 is detected using the second oscillation frequency f_{OSC2}.

Table V presents the effects of injected parametric faults on produced oscillation frequencies. The sensitivity of different oscillation frequencies with respect to a given injected fault changes depending on the relationship between the faulty component and the oscillation frequencies. To optimize the test procedure, redundant or nonefficient tests must be removed by identifying the most sensitive oscillation frequency for each injected fault. The most effective oscillation frequency is marked in Table V for each fault. It is interesting to note that, in the majority of cases, the output frequencies $f_{\mathrm{OSC3}}, f_{\mathrm{OSC4}}$, and f_{OSC5} are less sensitive than $f_{\mathrm{OSC1}}, f_{\mathrm{OSC2}}$, and f_{OSC6}. In other words, $f_{\mathrm{OSC3}}, f_{\mathrm{OSC4}}$, and f_{OSC5} do not cover any fault that cannot be covered by $f_{\mathrm{OSC1}}, f_{\mathrm{OSC2}}$, and f_{OSC6}. Therefore, the oscillation frequencies $f_{\mathrm{OSC3}}, f_{\mathrm{OSC4}}$, and f_{OSC5} can be eliminated to

TABLE V
PRACTICAL RESULTS OF THE INJECTED PARAMETRIC FAULTS IN THE MYOELECTRICAL AMPLIFIER/FILTER CIRCUIT; CATASTROPHIC FAULTS ARE NOT PRESENTED IN THIS TABLE

Fault	Oscillation Frequency Deviation						Fault	Oscillation Frequency Deviation					
	f_{OSC1}	f_{OSC2}	f_{OSC3}	f_{OSC4}	f_{OSC5}	f_{OSC6}		f_{OSC1}	f_{OSC2}	f_{OSC3}	f_{OSC4}	f_{OSC5}	f_{OSC6}
R₁(20%↓)	-4%	-5.5%	-6.5%	-7.8%	NI	NI	R₄(50%↓)	-7.8%	-3.5%	NI	NI	-14%	-41%
R₁(20%↑)	3.9%	7%	6.2%	7%	NI	NI	R₄(50%↑)	6.5%	4%	NI	NI	12%	NO
R₁(50%↓)	-8%	-13%	-13%	-14%	NI	NI	R₅(20%↓)	4.9%	29%	NI	NI	8%	10.7%
R₁(50%↑)	5.5%	14.5%	11.5%	12%	NI	NI	R₅(20%↑)	-3.5%	-19%	NI	NI	-6%	-23%
R₂(20%↓)	3.9%	9.5%	7.4%	7.5%	NI	NI	R₅(50%↓)	9.9%	97%	NI	NI	20%	31%
R₂(20%↑)	-4.5%	-5%	-6%	-6%	NI	NI	R₅(50%↑)	-5.5%	-35%	NI	NI	-9.8%	-22%
R₂(50%↓)	8.3%	24.8%	20%	19.9%	NI	NI	C₁(20%↓)	29.5%	NI	29.3%	NI	29%	NI
R₂(50%↑)	-7%	-13%	-11%	-12%	NI	NI	C₁(20%↑)	-19%	NI	-19%	NI	-19%	NI
R₃(20%↓)	27%	8.5%	28%	27%	28%	NO	C₁(50%↓)	101%	NI	100%	NI	100%	NI
R₃(20%↑)	-19%	-4%	-19%	-20%	-19%	-40%	C₁(50%↑)	-35%	NI	-35%	NI	-35%	NI
R₃(50%↓)	103%	15.5%	103%	103%	102%	NO	C₂(20%↓)	1.2%	27.6%	NI	NI	0.8%	-31%
R₃(50%↑)	-35%	-5.6%	-35%	-35%	-35%	-55%	C₂(20%↑)	-1.5%	-19%	NI	NI	-1%	NO
R₄(20%↓)	-3.8%	-2.5%	NI	NI	-6.5%	-35%	C₂(50%↓)	1.6%	94.5%	NI	NI	1.1%	-31%
R₄(20%↑)	4.2%	1.5%	NI	NI	6.2%	NO	C₂(50%↑)	-2%	-35%	NI	NI	-1.5%	NO

NO: No oscillation, NI: Not involved in the test.

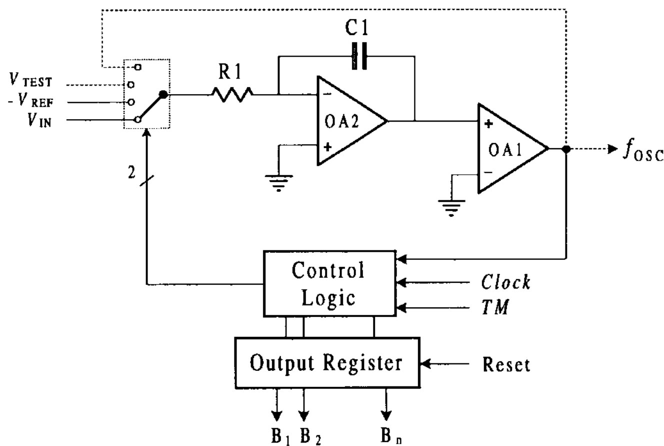

Fig. 7. Block diagram of a testable dual-slope ADC system based on the oscillation-test method ($R_1 = 50$ kΩ, $C_1 = 30$ pF).

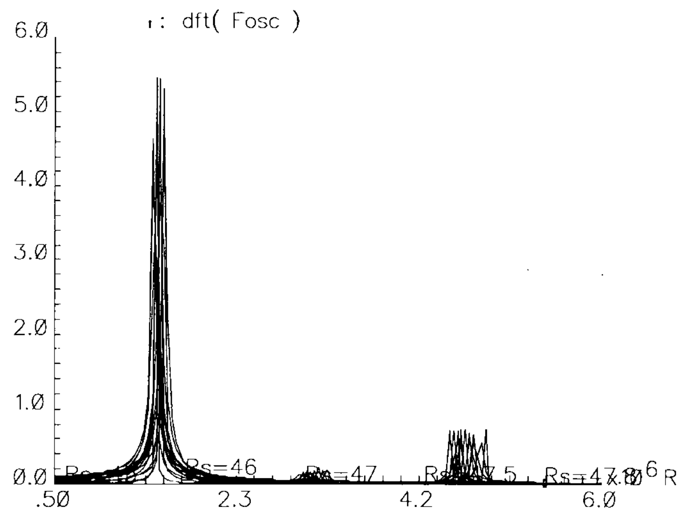

Fig. 8. FFT of the oscillation frequency of the dual-slope ADC in the test mode resulting from Monte Carlo analysis.

minimize the test procedure. As all remaining oscillation frequencies are observed at the output of OA2, the test point taken out from the output of OA1 is eliminated, and therefore only one test point is sufficient to monitor 100% of injected catastrophic and parametric faults in this example. The tolerance bands of oscillation frequencies f_{OSC1}, f_{OSC2}, and f_{OSC6} are determined to be [−4.5%, +6%], [−4.2%, +5.5%], and [−7.5%, +3%], respectively.

E. Dual-Slope ADC Testing

The test strategy proposed in this note has been applied to a dual-slope analog-to-digital converter (ADC) system as an example of a more complete mixed-signal circuit. A block diagram of a dual-slope ADC is shown in Fig. 7, in which the dotted lines are used only during the test mode (TM). The analog part of the converter comprises an integrator and a comparator. The property of integrating the input signal makes this converter immune to noise. The main advantage of this architecture over the single-slope ADC is that it eliminates the dependency of the conversion process on the linearity and accuracy of the slope. In this structure, it is necessary for $V_{\rm IN}$ to be positive.

At the beginning, the integrator is reset, and then the input switch selects $V_{\rm IN}$ which is integrated negatively for $N_{\rm REF}$ number of clock cycles. At the end of $N_{\rm REF}$ counts, the input switch selects $-V_{\rm REF}$, and the integrator integrates positively with a constant slope because $-V_{\rm REF}$ is constant. A counter counts until the comparator input crosses zero, which activates the comparator (OA1), and the counter is stopped. Hence, the actual counter content $N_{\rm OUT}$ numerically represents the analog input $V_{\rm IN}$ as follows:

$$N_{\rm OUT} = N_{\rm REF}\frac{V_{\rm IN}}{V_{\rm REF}}. \tag{11}$$

The test procedure is composed of two phases. In the first test phase, the input switch selects the output of the comparator to connect it to the input of the integrator to form an oscillator. Therefore, the oscillator is formed by the integrator and comparator without

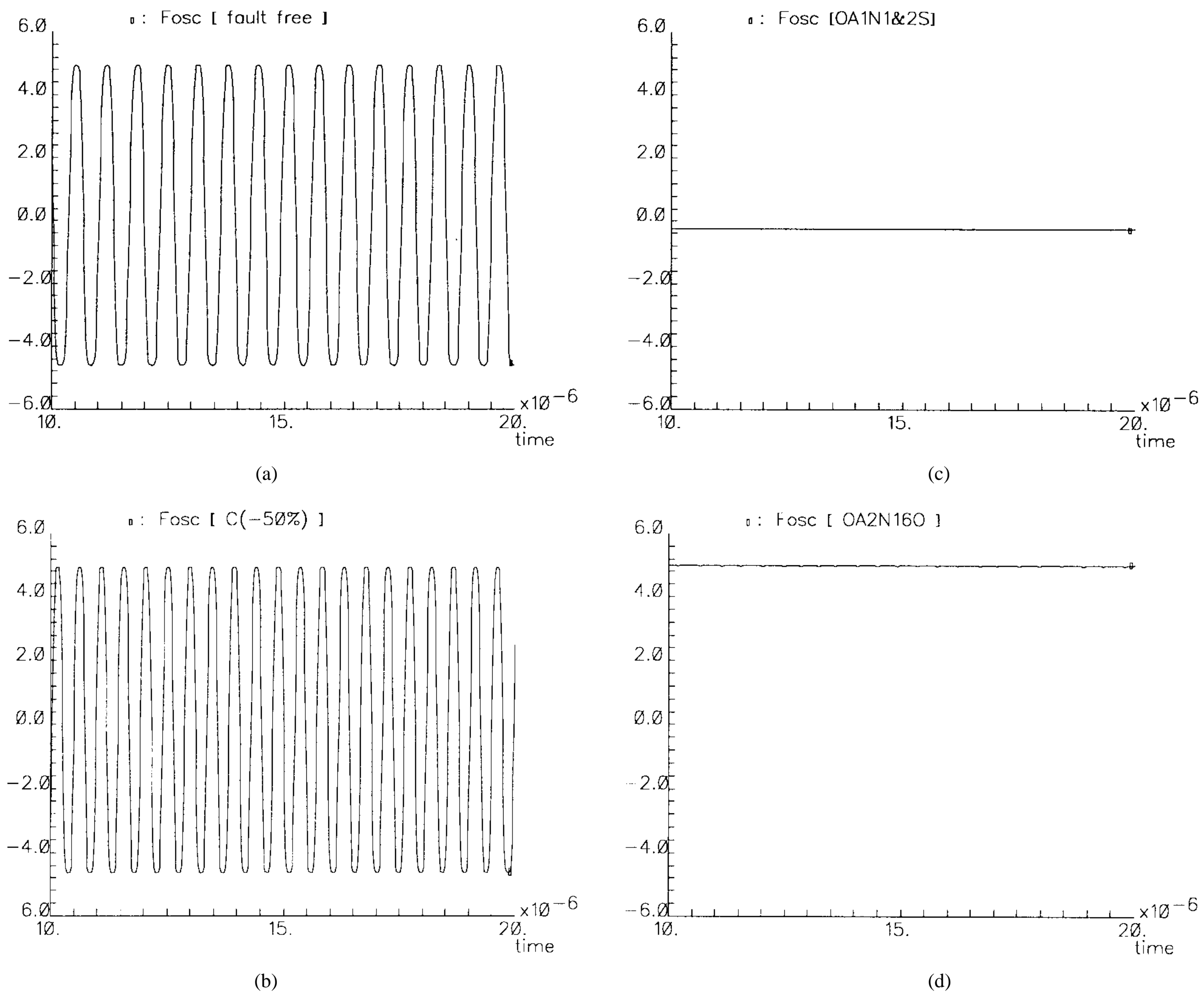

Fig. 9. Dual-slope ADC's output signal in the test mode without fault and in the presence of some typical injected faults (OA1N1&2S: short circuit between nodes 1 and 2 of OA1; OA2N16O: open circuit at node 16 of OA2). The oscillation frequency of the fault-free ADC is 1.53 MHz. Fault in the capacitor C_1 $[-50\%]$ deviates the oscillation frequency to 2.15 MHz.

any additional circuitry. The oscillation frequency is converted to a number by the counter existing in the control logic. The number obtained is compared with a predetermined test signature to verify whether or not there is a fault in the analog part of the ADC.

Note that all analog circuitry of the ADC are involved in the oscillator. In the second test phase, the ADC is rearranged to its functional mode, and a voltage reference (V_{TEST}) is converted to its corresponding digital word. The digital number is compared with the second test signature to verify the accuracy of the V_{REF}. All operations are directed by the control logic. In this way, the internal ADC blocks which contribute to the oscillator structure are tested. The simplicity and efficiency of this test architecture are obvious. The area overhead is related to only a small part of the control logic and a feedback loop.

The test time is very short because the test is performed in two phases, equivalent to the time needed to convert two analog signals using the ADC under test. Although this test partially verifies the functionality of the digital part, it is generally assumed that the digital circuitry already has been tested using the BIST method dedicated to the digital part of the chip.

A Monte Carlo analysis taking into account all process and design variations has been performed to determine the tolerance band of the oscillation frequency for fault-free ADC. To better visualize the tolerance band of the oscillation frequency, the fast Fourier transform (FFT) of the oscillating signal is presented in Fig. 8. The tolerance band is determined to be $[-4\%, +5.2\%]$.

Faults which deviate the oscillation frequency out of this tolerance band are considered to be detectable. The result of a comprehensive catastrophic fault simulation for the first test phase is presented in Table VI. The majority of injected faults resulted in loss of oscillation. For the sake of simplicity, the faults resulting in a loss of oscillation are not presented in the table. The shadowed faults cannot be detected in this test phase. The fault coverage of the first test phase is about 96.5%.

The second test phase increases the fault coverage to 98%. Fig. 9 illustrates the output signal of the dual-slope ADC in test mode without fault and for some typical injected faults.

IV. Fault Coverage

For all case studies presented in this note, a comprehensive list of hard faults has been inducted. The results confirm that high fault coverage can be achieved by only output frequency value evaluation for all cases.

The reason for this high fault coverage lies in two facts.

1) Operational amplifiers have at least two stages of amplification, which results in a very high gain. In the majority of applications, a

TABLE VI
COMPREHENSIVE LIST OF CATASTROPHIC FAULTS IN OA1 AND OA2

Fault	Oscillation Frequency Deviation	Fault	Oscillation Frequency Deviation
OA1N6,8-S*	+ 11%	OA1N28-O*	+ 274%
OA1N10,11-S*	- 8 %	OA2N1-O	- 4 %
OA1N31,32-S*	- 10 %	OA2N3-O	- 3 %
OA1N5,15-S*	+ 28%	OA2N6,8-S*	- 3 %
OA1N28,29-S*	- 2 %	OA2N9,11-S*	- 15 %
OA1N1-O	+ 7%	OA2N10,11-S*	- 3 %
OA1N3-O	+ 6%	OA2N28,29-S*	+ 2%
OA1N16-O	- 65 %	OA2N28-O*	+ 14%
OA1N18-O	- 54 %	***Other hard faults***	***No oscillation***

OA1N16-O: Open at the node 16 of the OA1, OA1N6,8-S: Short between nodes 6 and 8 of the OA1, *: Representing a set of schematically redundant faults.

feedback loop is added to establish the gain to a small but stable value which causes the redundancy in the OA-based analog circuits. In that case, the faults which decrease the open loop gain by a factor of 2, for example, will not affect the OA-based circuit performance. In the test structures presented in this note, the oscillation frequency depends directly on the intrinsic characteristics of the OA's, and therefore such a type of faults also can be monitored.

2) There are three sources of imprecision in analog testing: the imprecision related to the analog test vectors, the acceptable tolerance of the CUT, and the imprecision of voltage references and signature evaluations. During the test process, the acceptable performance deviation range must be enlarged to allocate these three sources of error because they may exist even if the CUT is fault free. In the OTS-based test structures, the first source of error is eliminated because no test vector is applied. The third error source is also minimized because the reference value is normally a frequency rather than a voltage which is easily converted to a number without significant precision degradation.

3) In a given oscillator, the oscillation frequency depends on a wide range of the ac behavior of its transfer function with variable sensitivities. For example, in a bandpass-based oscillator explained in this note, the oscillation frequency depends on the entire range of its open-loop ac behavior having greater than unity gain. In fact, the oscillation frequency can be considered as the sum of frequency components which can pass through the bandpass system with an amplification. Therefore, a change in any of these components will affect the oscillation frequency. When testing this bandpass system with a specified test frequency, based on conventional test methods, reliable information about the ac behavior of the rest of the transfer function cannot be achieved. In practice, many test frequencies should be applied to assure complete coverage over the ac behavior of the CUT. The sum of these test frequencies can be applied to the bandpass system as a multitone test frequency. In this case, the ac behavior coverage is comparable to the coverage obtained by the evaluation of the oscillation frequency in the oscillation-test strategy.

As the results indicate, the quantity of information about the CUT can be increased by simultaneous frequency and voltage level value evaluation of the output oscillation frequency or by applying the FFT technique to analyze the output oscillating signal.

V. CONCLUSION

A new vectorless dynamic test strategy based on converting the CUT to a circuit which is easier to test has been proposed. Its advantages, high fault coverage, reduced test time, a very simple test procedure, and the elimination of a test vector process, can be enumerated. Besides, its output signal can be evaluated precisely using pure digital circuitry. This test technique eliminates the need for costly specification tests, and can also be used to develop practical BIST techniques because no complicated circuit overhead is required. The oscillation-test method has been successfully applied to many typical analog and mixed-signal building blocks. Simulation results, obtained using CMOS 1.2 μm technology, and practical discrete realizations confirm the robustness of the proposed test strategy. The idea of producing and optimizing a set of oscillation frequencies to improve the fault coverage has been introduced. These results show that the oscillation-test method is very promising for analog and mixed-signal testing. In order to increase the efficiency of the oscillation-test method and to reduce the performance degradation due to test switches, the testability must be considered early during the design process. More design for testability techniques to transform other types of analog and mixed-signal circuits to an oscillator should be developed.

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A Fast Algorithm for Minimizing the Elmore Delay to Identified Critical Sinks

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***Abstract*—A routing algorithm that generates a Steiner route for a set of sinks with near optimal Elmore delay to the critical sink is presented. The algorithm outperforms the best existing alternative for Elmore-delay-based critical sink routing. With no critical sinks present, the algorithm produces routes comparable to the best previously existing Steiner router. Since performance-oriented layout generators employ iterative techniques that require a large number of calls to the routing algorithm for layout evaluation, a fast algorithm for routing is desirable. The algorithm presented here has a fast ($O(n^2)$, where n is the number of points) and practical implementation using simple data structures and techniques.**

I. Introduction

As minimum feature size decreases and circuit size and complexity increase, wire delay becomes the dominant component of circuit delay. The interconnect delay is the *RC* delay introduced due to the capacitance and the resistance of the metal wires connecting the source and the sink of the routing net. The Elmore delay model [11] has been shown to be a very accurate model for characterizing the *RC* interconnect delay of a routing tree [2], [15]. Earlier approaches using the minimum rectilinear Steiner tree [14], [7], [12], [5] minimize the total length of the routing tree. However, they may result in long delays between the source and the critical sink.

A routing algorithm is often used in the iterative refinement process of layout exploration for estimating the interconnect characteristic of a given configuration. After the placement of the modules is finalized, detailed routing is employed to actually perform the routing. During the iterative process, the routing, placement, and other optimization techniques are applied in a feedback loop until the layout converges to an acceptable solution. The time criticality of the routing tree and the placement of the pins are the feedback information given to a routing algorithm. Depending on the level of analysis, the feedback may be the criticality of a net as a whole, identified critical sinks in the net, or a time bound given to each sink in the net. Based on the availability of the feedback information, different criteria may be used for routing.

Manuscript received May 18, 1995; revised February 19, 1997 and July 28, 1997. This paper was recommended by Associate Editor G. Zimmermann.

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Publisher Item Identifier S 0278-0070(97)07655-0.

If the feedback information does not identify any sink as the critical sink, then the routing algorithm can either minimize the maximum delay to any sink in the net (radius), or minimize the average delay to all the sinks. Cong *et al.* [9] and Cohoon *et al.* [8] first proposed performance-oriented routing using a linear delay model. Both of these approaches considered the problem of minimizing the radius or the maximum delay to any sink of the routing tree. Alpert *et al.* [1] combined Kruskal's MST construction and Dijkstra's shortest path construction to generate better global performance-driven routing which minimizes the radius of the net. In [10], the authors formulate performance-driven routing along with wire sizing for minimizing distributed *RC*-tree delay. Their formulation also revealed the importance of minimizing both the radius and the total length of the tree. Recently, Vittal *et al.* [18] developed a performance oriented routing algorithm using alphabetic trees with $O(n^2)$ time complexity. Their approach is based on a global routing strategy that minimizes the average Elmore delay to all of the sinks.

If the feedback information to the routing algorithm identifies the critical paths in the circuit (i.e., identifies the critical sink in a net), then the routing heuristic should concentrate on minimizing the interconnect delay to the identified critical sink. In [16] Lim *et al.* gave an algorithm for minimizing the delay to identified critical sinks (POMRST algorithm) using a linear delay model in which they minimize a combination of the total tree length and the source-to-sink distance, based on Prim's MST construction. Their algorithm has $\Theta(n^3)$ time complexity. Hong *et al.* [13] also proposed timing-driven routing based on the wire delay model of [17] as the upper bound on the delay.

Both of these algorithms for critical sink routing are based on a linear delay model. As pointed out in [4], the topology of the tree has a significant effect on the critical sink delay, and hence a linear model based only on the tree length and the source-to-sink distance is inaccurate. Boese *et al.* [4] developed a routing heuristic for minimizing the Elmore delay to the identified critical sink (SERT-C). They first connect the critical sink to the source with minimum length wire, and then grow the Steiner tree for the rest of the sinks in a manner similar to Prim's algorithm, using the current Elmore delay to the critical sink as the cost criterion to be minimized. So far, the SERT-C algorithm is the most practical approach for critical sink routing reported in the literature. The SERT-C route, however, is often far from optimal, as will be illustrated with examples presented in this note. Their algorithm has an asymptotic time complexity of $O(n^2)$ where n is the number of nodes in the net. The authors of [3] developed a branch-and-bound algorithm to compute the routing tree with optimal Elmore delay to the identified critical sink (BBSORT-C) which they used to obtain optimal Elmore trees for small nets.

The performance-driven routing algorithm presented in this note also belongs to the class of routing algorithms where prior knowledge about the critical path in the circuit is utilized to reduce the critical path interconnect delay. The Elmore delay model is used directly to guide the construction of the routing tree. The algorithm is based on an efficient tree update heuristic presented in [5] which considers adding an edge to the existing tree as a replacement for another edge in the tree, resulting in an improvement in the cost criterion. The heuristic has a practical, $O(n^2)$, implementation using conventional data structures such as linear arrays and adjacency lists. Due to the ability of the heuristic to consider global improvements in the tree, the resulting routes generated by the algorithm presented here are far superior in quality as compared to [4]. Most existing automatic

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