Selective area growth of germanium and germanium/silicon-germanium quantum wells in silicon waveguides for on-chip optical interconnect applications

S. A. Claussen,* K. C. Balram, E. T. Fei, T. I. Kamins, J. S. Harris, and D. A. B. Miller

Department of Electrical Engineering, Stanford University, 350 Serra Mall, Stanford, CA 94305, USA
**stephanie.ann.claussen@gmail.com*

Abstract: We propose a robust fabrication process for growing Ge and Ge-based heterostructures in growth windows with Si sidewalls which can be applied to growth in thick Si optical waveguides. Sidewall growth is eliminated by the presence of a dielectric spacer layer which covers the sidewalls. We demonstrate the effectiveness of this process by selective-area growth of Ge and Ge/SiGe quantum wells, and show an improved performance and increased process reliability over previous work.

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1. Introduction

The ability to selectively grow germanium in specific regions of a silicon substrate is highly desirable for the future integration of Ge-based optoelectronice devices with high-speed Si-based electronic circuits. Potential applications include dense integration of high-performance photodetectors [1,2] and optical modulators [3,4]. While selective-area growth of Ge has been investigated since the mid-1980s [5], using these growth processes in the fabrication of actual devices often introduces additional challenges. For example, selective growth of Ge is commonly carried out by using a dielectric mask such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) above the Si substrate. Growth windows are etched through the dielectric and Ge growth is initiated at the exposed Si surface [1,6]. Certain device designs [3,4] require growth of a Ge region inside a Si optical waveguide, with the growth regions etched through the dielectric layer and into the underlying Si waveguide layer. Since any exposed crystalline silicon surface can serve as a growth template for the Ge, the exposed Si sidewalls initiate deleterious growth that affects both the optical and electronic properties of the device. In this work, we propose and demonstrate a fabrication process to reliably prevent growth on these Si sidewalls, even in relatively thick structures, and demonstrate highly selective growth of both Ge and SiGe.

Ge and Ge/SiGe quantum wells (QWs) both exhibit electroabsorption effects (the Franz-Keldysh effect in bulk Ge [7,8] and the quantum confined Stark effect (QCSE) in Ge/SiGe QWs [9]), where an increase in the applied electric field redshifts the absorption spectrum of the material. This behavior allows the development of compact, high-performance, Ge-based Si-compatible optical modulators for optical interconnect applications [10,11]. Waveguide-based modulators allow for longer interaction lengths between the optical beam and the active material and easier integration with other on-chip optical components. However, to minimize loss from background absorption in Ge structures, the modulator region must be integrated with low-loss entrance and exit waveguides, such as silicon-on-insulator (SOI) waveguides. These waveguides can be single-mode while still being relatively thick. Coupling between the active Ge region and the passive waveguide can be carried out either evanescently using adiabatic tapers [12] or through direct butt coupling [3]. In the case of adiabatic coupling, a Ge layer is grown directly above the Si layer of the SOI substrate. The adiabatic tapers used are typically very long, increasing the footprint of the device and, if formed out of the active Ge material, increasing the device capacitance. Growing the Ge or Ge/SiGe QWs in growth windows directly in the SOI waveguide, butt-coupling the modulation region to the input and output waveguides, enables a modulator with a small footprint and low capacitance. However, these growth windows can have very thick sidewalls of exposed Si (depending on the thickness of the SOI waveguide), where Ge growth is expected to occur if preventative steps are not taken.

This growth on the exposed Si sidewalls needs to be avoided because it can significantly disturb the planarity of the device, making post-growth fabrication and integration with other devices difficult or requiring chemical mechanical polishing (CMP). Planarity is also important for the optimal performance of heterostructures like QWs. Furthermore, for active devices that rely on *pn* or *p-i-n* junctions that are doped *in situ* during growth, growth on the sidewalls can lead to electrical shorting of the device or high leakage current.

2. Design motivation

To prevent sidewall growth and enable high-quality growth in the desired regions, a process was previously proposed to deposit a dielectric spacer on the sidewalls of the growth windows [13]. Figure 1(a) shows a schematic of the designed substrate, with Ge/SiGe QW growth in the growth window of an SOI waveguide. (It should be noted that while much of the discussion here focuses on integration with 3 μm-thick SOI waveguides because this is the desired application, the results transfer completely to applications that require selectively growing in growth windows etched into bulk Si substrates or SOI waveguides of different thicknesses. In fact, much of the development of this work and the results shown here were

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done using Si substrates.) Unfortunately, while this previously proposed spacer fabrication process did allow the demonstration of high-quality QW growth, it was not robust to minor fabrication variations, making mode-matched growth with SOI waveguides unreliable. Figure 1(b) presents a typical result, with excessive sidewall growth visible and planar QW growth at the center of the growth window. Despite many efforts to modify this fabrication process, it proved to be very sensitive to minor process variations, which led to poor repeatability and yield. A weak point in the approach was determined to be at the top corner of the Si sidewall, directly under the SiO_2 growth mask. The dielectric spacer was likely removed from this corner during a dry etching step in the substrate fabrication, if the spacer layer at this corner was not sufficiently protected during the etch by the top SiO_2 mask.

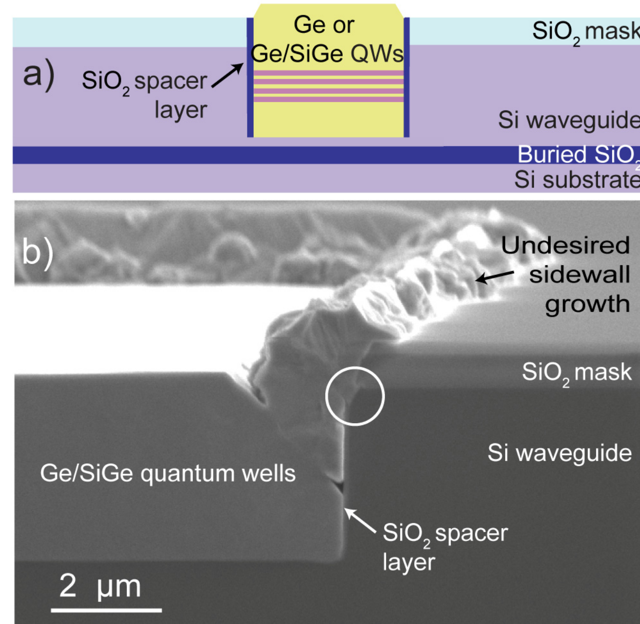

Fig. 1. (a) Desired growth results using the substrate preparation process suggested by Ren *et al.* [13]. (b) Scanning electron microscope (SEM) image of selective area growth of Ge/SiGe QWs. Implementation of the spacer fabrication process proved to be not very robust, and often resulted in undesired sidewall growth originating from the top corner of the Si sidewall, directly under the SiO_2 mask edge (circled region). The dielectric spacer was likely removed from this corner during a dry etching step in the substrate fabrication, due to insufficient coverage of the spacer by the top SiO_2 mask.

To overcome this problem of unreliable spacer fabrication and thus substantial sidewall growth, we propose a change in the original spacer fabrication process set forth by Ren *et al.* [13] that renders it independent of process variations. When determining a potential fabrication process for the spacer, a few considerations need to be kept in mind. First, it is desirable to make the spacer as thin as possible, to minimize optical loss [13]. The spacer needs to also be formed only on the vertical sidewalls of the growth window, not at the bottom of the window, where the epitaxial growth is initiated. Finally, great care needs to be taken so that the spacer fabrication does not damage this growth surface at the bottom of the window.

3. Fabrication process

Figure 2 illustrates the new proposed process. Beginning with either a Si or SOI wafer, the SiO_2 growth mask is formed through thermal oxidation or through deposition of low-temperature oxide (LTO) via low-pressure chemical vapor deposition (LPCVD). If this latter option is used, the LTO is densified at 1100°C for 1 hour to reduce the number of dangling

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bonds present; any such dangling bonds likely contribute to undesired growth nucleation on the top SiO_2 surface. We found that using thermal SiO_2 or densified LTO as the growth mask give comparable selectivity results under the growth conditions used here. Then, the growth windows are patterned using standard photolithography. The top SiO_2 layer is etched using a CHF_3/O_2 reactive ion etch (RIE). Then, the Si is etched using a timed $HBr/Cl_2/O_2$ RIE etch to the desired depth. Because this process was designed for use on an SOI substrate with a 3 µm-thick Si device layer, the growth windows were etched ~2.8 µm into the Si, to allow a sufficiently thick remaining Si layer (~200 nm) to initiate epitaxial growth. The process up to this point (Step 3 in Fig. 2) is identical to that adopted in the previous process shown in Fig. 1.

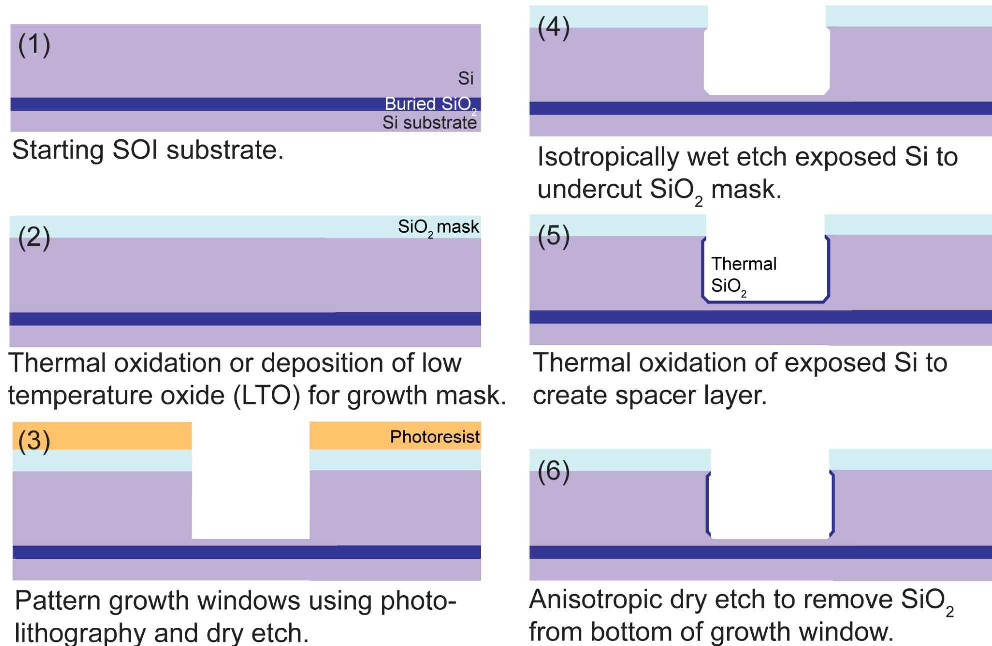

Fig. 2. Proposed new dielectric spacer fabrication process. The SiO_2 spacer on the sidewalls is protected by the overhanging SiO_2 mask layer, preserving it during subsequent fabrication steps and ensuring that the sidewall remains completely covered.

In our new process, however, following removal of the photoresist, the Si device layer is etched in a wet etchant to undercut the Si sidewalls. Room temperature tetramethylammonium hydroxide (TMAH) was used here. As shown in Fig. 3, the undercut can be controlled by the etch time used. Following this wet etch, the wafer is thermally oxidized to form the SiO_2 spacer layer. The simulations by Ren *et al.* show that optical reflections and scattering off this spacer layer decrease as the thickness of the SiO_2 layer decreases [13]. Thus, the spacer should only be as thick as is necessary for full coverage of the sidewall. In this work, we targeted a final spacer thickness of 80 nm, which Ren *et al.* predict will transmit about 80% of the optical power [13]. This thermal oxidation step also serves to remove damage to the Si surface at the bottom of the growth window that may have occurred during dry etching of this region.

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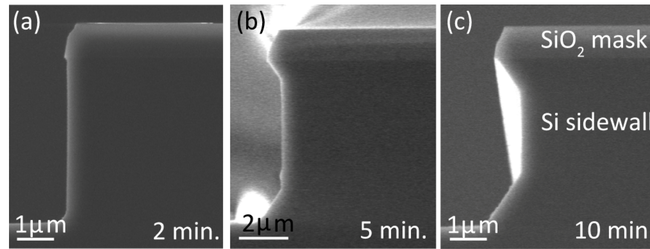

Fig. 3. Longer wet etch times of the Si sidewalls lead to greater amounts of undercut, as shown by these cross section SEM images of samples that were etched for (a) 2 minutes, (b) 5 minutes, and (c) 10 minutes. The wet etch used in this work, tetramethylammonium hydroxide, etches different crystal planes of Si at different rates, resulting in the faceting evident at longer etch times.

Finally, an anisotropic dry etch followed by a very short wet etch in 20:1 buffered oxide etch (BOE) are used to remove the thermal SiO_2 from the bottom of the growth window while leaving it on the sidewalls. The key to the success of this process is the presence of the overhanging SiO_2 growth mask, which serves to protect the spacer on the sidewalls from being etched while the SiO_2 layer at the bottom of the growth window is dry etched. During the subsequent selective buffered oxide wet etch, the thickness of the SiO_2 at the bottom of the growth window is much less than that on the sidewalls. Thus, the bottom of the growth window can be completely cleared of SiO_2 while a continuous layer is maintained on the sidewalls, including at the top edge of the Si sidewall directly under the SiO_2 growth mask layer, which was a weak point in the previous process design of Fig. 1.

4. Epitaxial growth conditions

In this work, both Ge/SiGe quantum well samples and pure Ge samples were epitaxially grown on either a Si(001) substrate or a silicon-on-insulator substrate (with a 3 μm Si device layer and 375 nm buried oxide layer) in an Applied Materials Centura reduced-pressure chemical vapor deposition (RPCVD) reactor. The growth process used GeH_4 and SiH_4 in a H_2 carrier gas at a temperature of 405°C and a system pressure of 40 Torr. No HCl was added to the process gases so selectivity was not optimal. To decrease the defect density and surface roughness, the quantum wells were grown on p-type $Si_{0.12}Ge_{0.88}$ buffer layers (*in situ* doped with boron) that underwent high temperature hydrogen annealing; the pure Ge samples also undergo multiple hydrogen anneals for heteroepitaxy (MHAH) [9,14]. To prevent dopant diffusion into the quantum wells, a layer of intrinsic $Si_{0.12}Ge_{0.88}$ was grown both before and after the quantum well region. The absorbing region consisted of 20 quantum wells which were 15 nm wide with 35 nm barriers and a top capping layer of *n*-type, arsine-doped $Si_{0.12}Ge_{0.88}$.

5. Results and conclusion

As shown in Fig. 4, this altered design reliably leads to high-quality Ge growth with minimal sidewall growth. For this result, a 5 minute TMAH wet etch was used, to ensure an adequate undercut of the Si sidewall while not greatly distorting the profile of the interface between the Si waveguide and the Ge modulation region.

Crystal faceting at the sidewalls, which has been observed in other selective-area growth work [1,6], is evident and points to well-controlled and high-quality growth. This faceting is believed to be due to different crystal planes of Ge or SiGe growing at different rates, depending on the growth temperature used [6]. Furthermore, the process developed here is simpler than the previously proposed one, with fewer process steps. This fact, combined with the robustness that is built into the process design due to the presence of the overhanging SiO_2 masking layer, leads to much higher yields.

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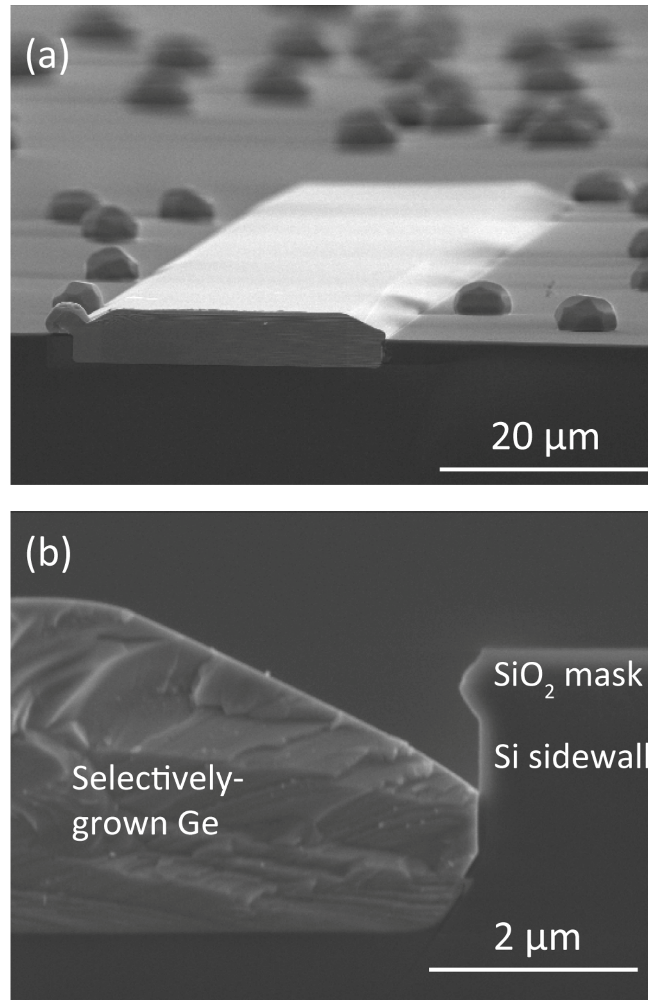

Fig. 4. SEM images of selective-area Ge growth using the dielectric spacer fabrication process in Fig. 2. (a) Angled image of a sample etched in TMAH for 5 minutes. Ge nucleation is evident on the top surface of the SiO_2 mask, indicating imperfect selectivity. (b) Cross section SEM showing Ge crystal facets at the edge of the growth window.

Random nucleation of the Ge growth occasionally occurred on the oxide-covered sidewalls and the top oxide growth mask, as seen in Fig. 4. (This nucleation was also present when the previous substrate fabrication process was employed, though it cannot be observed in Fig. 1 due to the smaller SEM window of that image.) The density of growth nucleation varies, as the area of these clusters increases with increasing growth times. With the thick 2-5 μm growths used in this work, the nucleation would typically cover less than 10% of the surface area of the top oxide growth mask. We expect such nucleation could occur especially at broken bonds on the oxide surface. Thermally grown oxide or adequately annealed deposited oxide are expected to have a low density of broken bonds on the surface; this is the reason we perform a high temperature anneal following the initial deposition of the LTO growth mask. Great care is taken to repair any possible damage to this top oxide layer that may be incurred during the subsequent spacer fabrication process. Specifically, exposure to a plasma during dry etching can break bonds and provide growth nucleation sites. Thus, following the final dry etch step (Fig. 2 Step 6), a high temperature anneal is performed on the substrates (1050°C for 1 hour) to try to repair this dry etch damage to the oxide growth mask. However, as shown in Fig. 4, it was difficult to completely prevent this nucleation from

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occurring; this would require extensive development of new growth recipes, for example using HCl to inhibit nucleation, which was not carried out in this work.

In conclusion, we have developed and demonstrated a process for preparing substrates for selective-area epitaxial growth of Ge and Ge/SiGe QWs in growth windows etched into the Si substrate or Si waveguides. This fabrication process results in a thin dielectric layer completely covering the exposed Si sidewalls of the growth region, preventing Ge growth from occurring on the sidewalls and restricting it to only the bottom of the growth window, as desired. This process enables future integrated low-loss, high-performance Ge and Ge/SiGe QW waveguide modulators and photodetectors monolithically integrated with SOI waveguides.

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