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Novel Structures for a 2-Bit per Cell of Nonvolatile Memory Using an Asymmetric Double Gate

Kuk-Hwan KIM[†a)], **Hyunjin LEE**[†], ***Nonmembers***, ***and*** **Yang-Kyu CHOI**[†], ***Member***

SUMMARY A 2-bit operational metal/silicon-oxide-nitride-oxide-silicon (MONOS/SONOS) nonvolatile memory using an asymmetric double-gate (ASDG) MOSFET was studied to double flash memory density. The 2-bit programming and erasing was performed by Fowler-Nordheim (FN) tunneling in a NAND array architecture using individually controlled gates. A threshold voltage shift of programmed states for the 2-bit operation was investigated with the aid of a SILVACO® simulator in both sides of the gate by changing gate workfunctions and tunneling oxide thicknesses. In this paper, the scalability of the device down to 30 nm was demonstrated by numerical simulation. Additionally, guidelines of the 2-bit ASDG nonvolatile memory (NVM) structure and operational conditions were proposed for "program," "read," and "erase."

key words: *MONOS, SONOS, Fowler-Nordheim tunneling, flash memory, asymmetric double gate, nonvolatile memory*

1. Introduction

High density nonvolatile memory (NVM) is in high demand in the mobile and mass storage media market due to low cost-per-bit needs. However, scaling down of the conventional NVM through use of a floating gate structure is expected to face 45-nm barriers due to a scaling limit in tunneling oxide thickness [1]. Solutions are being studied for the next generation NVM, such as the MRAM, FeRAM, Polymer Memory and Ovonic Unified Memory (OUM); but, these technologies are considered to be rudimentary [2]. Currently, there is no definite solution to extend scaling of the conventional NVM beyond the limited 45-nm technology node. A new NVM cell architecture is greatly needed to overcome technical challenges at this 45-nm node.

Two major mainstreams appear as the effort to search for short-term next generation NVM. First mainstream: memory cell structures employing discrete traps as the charge storage media have attracted a lot of research attention as the promising candidates to replace conventioanl floating gate NVM. The conventional floating gate NVM, which offers longer than ten years of retention time, has the drawbacks of high operation voltage and slow write/erase because of their relatively thick tunnel oxide. When stored in discrete traps, charges are more immune to the leakage caused by localized oxide defects, thus improving the device retention characteristics. Memories with discrete charge storage elements allow more aggressive scaling of the tunnel oxide and exhibit superior characteristics compared to conventional floating gate NVM in terms of operation voltage, write/erase speed, and endurance [3], [4]. Moreover, the discreteness of the charge traps enables multibit-per-cell storage without going through the multilevel approach, which poses stringent requirement on the control of spread of the threshold voltage [5]. The discrete charge storage elements utilized in such devices are usually traps in a nitride film [6], [7], or isolated Si, Ge or various metal nanocrystals.

Second mainstream: Multi-level cell or multi-bit cell nonvolatile memory is one of the most promising structures to not only increase the density, but to also circumvent the scaling problems. Multi-level cell, which offers lower bits per cost without any cell-structure changes, has the drawbacks of heavy decoder burden and lower program performance than the same denstiy single-level cell [8]. Memories with more than two discrete charge trapping storage regions enable multibit-per-cell memory. So far, even though the localized trapping NVM based on source/drain swapping operation has attracted a lot of research attention [9], it is expected to suffer from some dimensional effects such as inteference between charge trapping regions beyond 30 nm node. Recently, a novel 2 bit operational NVM based on individually controlled ASDG is proposed [10]. By selectively charging the front and the back gate of ASDG NVM four different gate bias conditions can provide the four programmed states: "00," "01," "10," and "11." Despite this functionality, insufficient details of how to fabricate and make them feasible from a process point of view dilute the strength of previous works.

In this paper, a NVM cell architecture based on an ASDG MOSFET with the details of process flow was proposed and studied as a breakthrough to the 45-nm barriers. The detail guidelines in adjusting the programmed threshold voltages were studied for various gate workfunctions and tunneling oxide thicknesses. Additionally, operational conditions of the ASDG NVM were verified and optimized with a 2-D SILVACO® simulator for "program," "read," and "erase."

2. ASDG NVM Structure

One of the key issues in considering a novel NVM is how to increase the program/erase speed to sustain good data retention characteristics. Unfortunately, in planar structures, it is very difficult to find an optimum tunneling oxide thickness for both a fast program/erase speed and a good retention

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[†]The authors are with Dept. of EECS, Korea Advanced Institute of Science and Technology, 373-1 Guseong-Dong, Yuseong-Gu, Daejon, Korea.
a) E-mail: modestpe@nobelab.kaist.ac.kr

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time due to the trade-off relationship between the two. To overcome the trade-off relationship between program/erase speed and retention time, an attractive option is the adoption of the FinFET structure with a reduced electric field to the gate oxide or the oxide-nitride-oxide (ONO) in SONOS memory. FinFET is a symmetric double-gate device, which allows the same scalability for the relatively thick gate dielectric thickness as compared to single-gate devices. Thus, a double gate structure like FinFET can provide an opportunity to use a thick tunnel oxide thickness while supporting good retention characteristics and maintaining the same scalability [11], [12]. With a simple change of conventional FinFET fabrication, ASDG can be fabricated. Addionationly memory characteristics can be obtained by using nitride film as charge trapping region.

2.1 The Details of ASDG NVM Structure

Figure 1 shows the cross-sectional views of the proposed ASDG NVM cell with different workfunctions of the front gate (FG) and back gate (BG) materials with an ONO (tunneling oxide/nitride/blocking oxide) structure. In this paper, a nominal structure for the simulation had a 30-nm gate length (L_G) with a 10-nm silicon film thickness (T_{si}) for the purpose of demonstrating the advancement beyond the 45-nm regime. To avoid direct tunneling of the stored charge, a 4-nm thickness of the blocking oxide was used [13]–[15]. A 5-nm thickness of the nitride was used to ensure sufficient traps for the charge storage [16]. For the purpose of optimizing operating time versus data retention, the tunneling oxide thickness was varied from 1 nm to 4 nm. The workfunction of the FG was varied from 3.6 eV to 4.6 eV and that of BG was varied from 4.6 eV to 6.2 eV, which was higher than that of the FG to obtain a simple programming mechanism.

The bits stored on the top and bottom nitride are referred to as bit1 and bit2, respectively. The logic "1" refers to the programmed bit and the logic "0" refers to the erased bit. To program bit1, a positive program bias was applied to the FG and electrons were captured at the tunneling oxide/nitride interface. To program bit2, a positive program bias was applied to the BG. The threshold voltage shift from state "00," i.e., no programmed state, was proportional to the amount of captured electrons in the nitride interface according to the bias condition of the FG and BG. The blocking oxide suppressed leakage of the trapped electrons from the nitride to the gate.

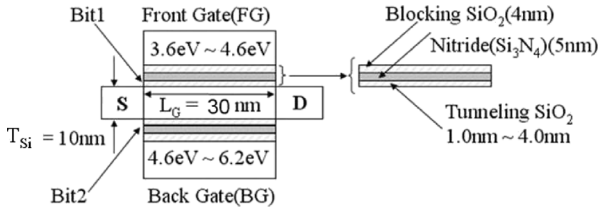

Fig. 1 Cross-sectional schematics of the ASDG NVM cell along a-a' in Fig. 2(c).

2.2 The Fabrication of ASDG NVM Structure

To provide 2-bit operation with one transistor, a novel struc-

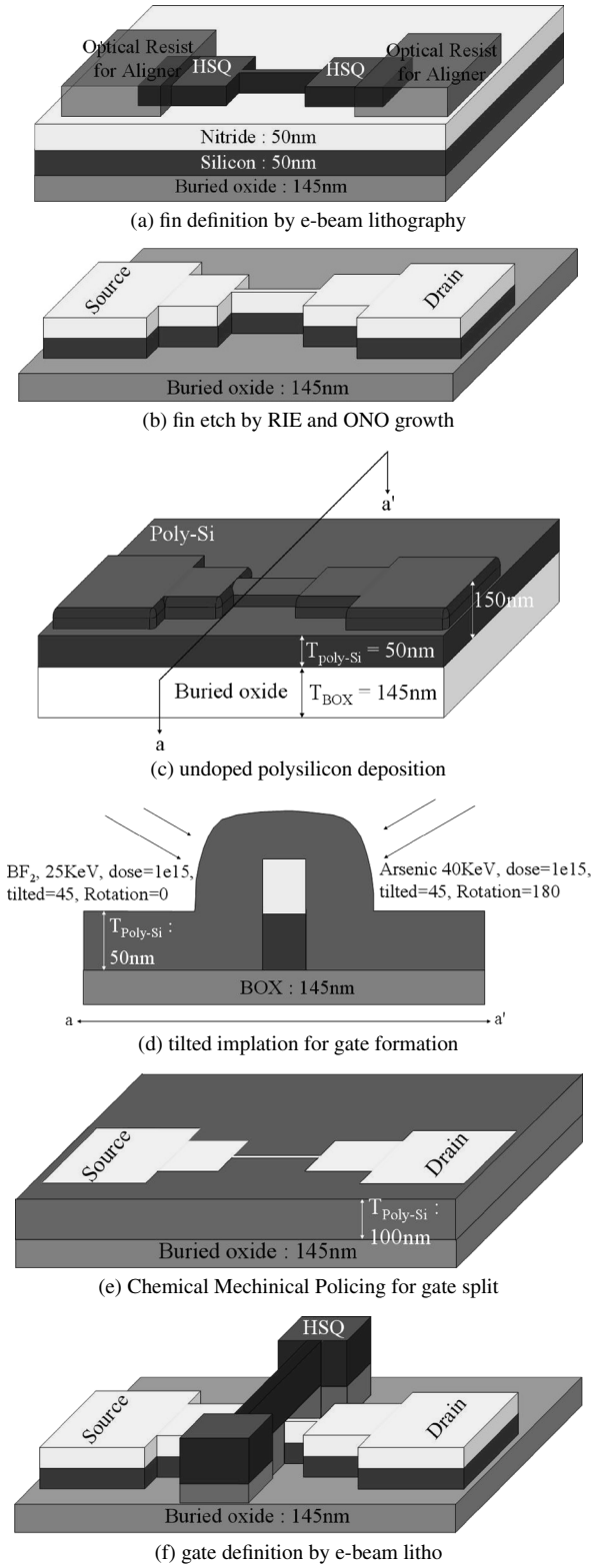

Fig. 2 Schematic diagrams of the proccess flow for a asymmetric FinFET SONOS device.

ture was modified from the original symmetric double-gate FinFET to the asymmetric double-gate. The fabrication flow is shown in Fig. 2. Starting SOI wafers contained a 145-nm buried oxide layer and a 100 nm lightly p-type doped device layer. With a repetitive oxidation and HF wet etching, thinning the SOI layer to 50 nm is performed. Nitride film of 50 nm thickness is deposited by LPCVD for CMP stopper. (a) Fin widths ranging from 20 to 100 nm are written using electron-beam lithography. The aspect ratio of fin width and fin height should be carefully determined so that one dopant in a gate can not cross over to the other side. (b) The capped nitride and SOI silicon are patterned by plasma etch to be served as a channel. A sacrificial SiO_2 is grown and removed to alleviate damaged sidewalls. An identical 2-nm thermal SiO_2 is grown for the gate dielectric. 5 nm of nitride film for charge trapping element and 4 nm of SiO_2 for blocking oxide are deposited by LPCVD respectively. (c) 50 nm of undoped polysilicon is deposited. (d) BF_2 is implanted with conditions of 25 keV, 10^{15} atoms/cm^2, and 45° tilt. And then, aresenic is implanted with conditions of 40 keV, 10^{15} atoms/cm^2, 45° tilt, and 180° rotation of wafer. The workfunction can be adjusted in the range from 4.1 eV to 5.2 eV by changing implanted dose, type, energy when using tilted implation. Figure 3 shows the simulated doping profile of the gate after tilted implantation with the aid of 2-D Athena simulator. (e) Additional 50 nm of undoped polysilicon is deposited and wafer is polished and planarized with CMP until the capped nitride is exposed in order to disconnect the N^+ corresponding to the FG and the P^+ gate corresponding to the BG. Both FG and BG can be biased individually, which is essential for the multi-bit operation. (f) A gate electrode is delineated by using the electron-beam lithography. Then, it was patterned by the plasma etch. By using the remained gate photoresist as an implant stopper, phorsphorous is implanted with the conditions of 40 keV, 10^{15} atoms/cm^2, and 0° tilt for source/drain formation, followed by 1000°C, 5 sec RTA.

Alternatively, a metal gate also can be used to achieve a wide range of workfunctions without using tilted implantation to the polysilicon. This idea can be realized by using the oblique sputtering of different metals consecutively. For example, one metal of a low workfunction was sputtered with a large tilted angle, then, following a 180° wafer rotation, another metal of a high workfunction was sputtered again. The final structure obtained using this oblique sputtering was identical to the structure produced by using N^+/P^+ polysilicon gate as well as CMP. The achievable workfunction by using various metal gates is arranged in Table 1.

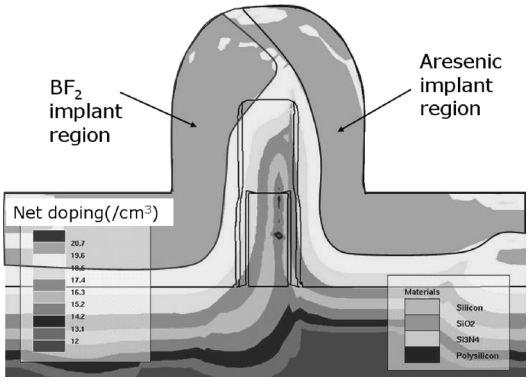

Fig. 3 Cross-section of ASDG FinFET along a-a' direction in Fig. 2(c) and shows the simulated doping profile after tilted implantation.

Table 1 The workfunctions of candidate metal gate electrodes.

Metal	Achievable workfunction [eV]	Type
Ti	3.95-4.33	N-type
Ta	4.12-4.25	N-type
Zr	3.9-4.05	N-type
Ni	4.5-5.3	Mid-gap
Pt	5.32-5.5	P-type
RuO_2	4.9-5.2	P-type

3. 2-Bit Operation of the Proposed Device

Figure 4 shows the transient characteristics of the trapped charge on the tunneling oxide/nitride interface at the front gate and the back gate side during programming. N^+ polysilicon was used for the front gate, and P^+ polysilicon was used for the back gate. The trapped charge at the back gate side in state "11" was smaller than that of the front gate in state "11," even though the programming condition of V_G = 15 V was applied to both gates. Because the workfunction of the back gate was larger than that of the front gate, the threshold voltage of the back gate was larger than that of the front gate. This meant that fewer electrons could pass over the tunneling oxide barrier at the back gate side as compared to the front gate side.

Figure 5 shows the energy band diagram of the SONOS device at the front gate side and back gate side during the programming, respectively. The energy bending between the tunneling oxide and silicon substrate was more severe at the n^+ poly gate side than the p^+ poly gate side. This was

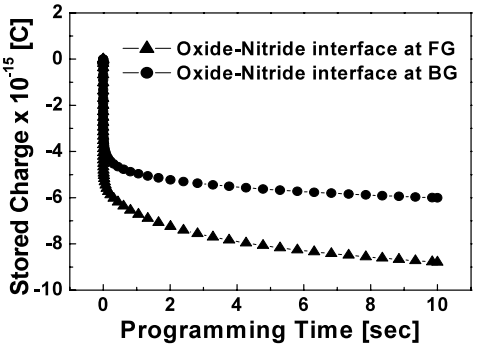

Fig. 4 The transient characteristics of the stored charge with $V_{FG} = V_{BG}$ = 15 V on the nitride interface for states "11."

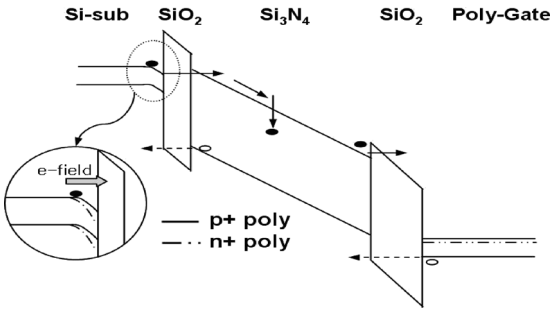

Fig. 5 The energy band diagram of the SONOS device during programming.

due to the difference of the Fermi level between the n^+ poly gate and silicon substrate being higher than that between the p^+ poly gate and silicon substrate. More energy bending makes a higher electric field, so more charges could acquire the energy to cross over the SiO_2 potential barrier at the n^+ poly gate side than the p^+ poly gate side.

4. The Optimization of the Proposed Device

In multi-bit memory, a reading voltage was applied to both gates to determine the programmed state. Due to the different threshold voltages of each programmed state, distinguishable current values were measured proportionately even though the same bias was applied to the both gates. For proper operation in the multi-bit cell, a wide threshold voltage window among the programmed states is of high demand.

Figure 6 shows a reading current at different states with 4.1 eV for the front gate workfunction (WF_{FG}) and 5.2 eV for the back gate workfunction (WF_{BG}). In Fig. 6, it is more crucial to make a wide sensing window between "00" and "01," as well as between "01" and "10," than between "10" and "11."

The threshold voltage shift in "program" operation was used as the current window for the optimized process. The threshold voltage (V_T) was defined as a gate voltage read at the 100 nA drain current with V_{DS} =50 mV. $V_{T,00}$, $V_{T,01}$, $V_{T,10}$ and $V_{T,11}$ represent threshold voltages of the programmed states "00," "01," "10" and "11," respectively. Additionally, the threshold voltage difference between adjacent states should be larger than 0.8 V for reliable 2-bit operation.

4.1 The Optimization of Gate Workfunction

Figure 7 and Fig. 8 show the threshold voltage shift among the adjacent four types of programmed states for various gate workfunctions. Figure 7 shows that $V_{T,10}$–$V_{T,01}$ increased as the WF_{FG} decreased with the fixed 5.2 eV for the WF_{BG}. Corresponding to a reduction in WF_{FG}, more electrons were trapped in the nitride interface of the FG side due to the lower barrier. Because the electric field from the FG to the channel was disturbed by the trapped electrons in the nitride interface, V_T,10 increased. This resulted in increasing

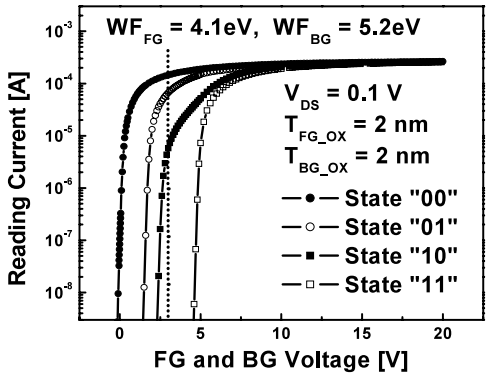

Fig. 6 I-V characteristics of the ASDG cell programmed with the 4 distinguishable states of "00," "01," "10," and "11."

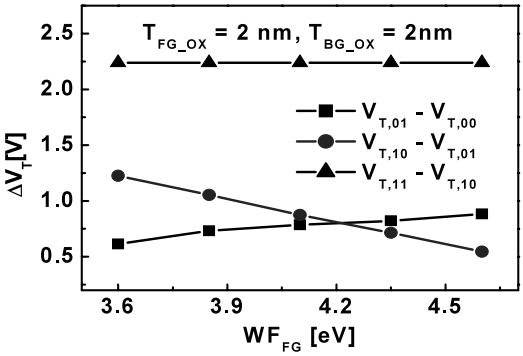

Fig. 7 A shift of threshold voltage for various front gate workfunctions.

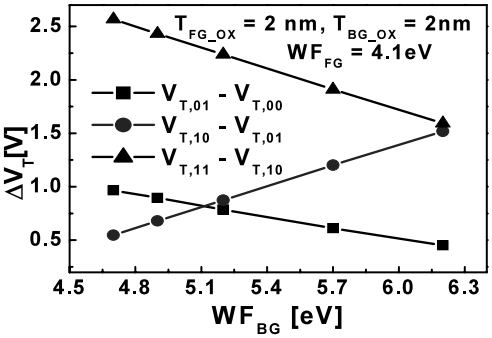

Fig. 8 A shift of threshold voltage for various back gate workfunctions.

of $V_{T,10}$–$V_{T,01}$. Figure 8 shows that $V_{T,01}$–$V_{T,00}$ decreases, and $V_{T,10}$–$V_{T,01}$ increases as the WF_{BG} increases with the fixed 4.1 eV for the WF_{FG}. Similarly, these results are attributed to the reduction to trapped electrons in the nitride interface due to the higher barrier height as the WF_{FG} increased. A trade-off exists between V_T,10–V_T,01 and V_T,01–V_T,00 because of the decreased V_T,01. From Fig. 7 and Fig. 8, 4.1 eV and 5.2 eV were chosen as the optimized values of the WF_{FG} and WF_{BG} so that all the threshold voltage differences between adjacent states should be larger than 0.8 V.

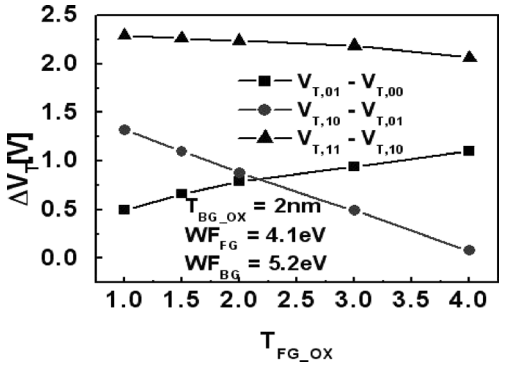

Fig. 9 A shift of threshold voltage for various front gate oxide thicknesses.

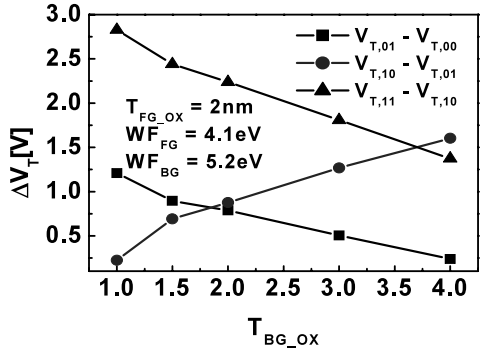

Fig. 10 A shift of threshold voltage for various back gate oxide thicknesses.

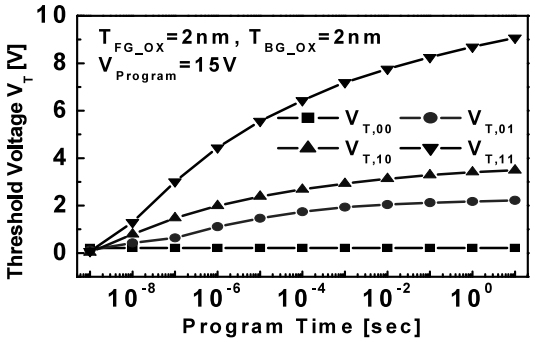

Fig. 11 Transient behaviors of the V_T during the erase operation.

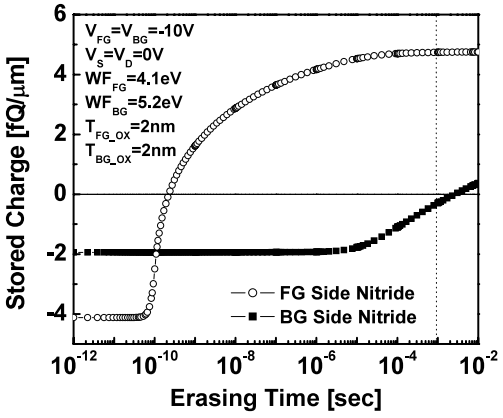

Fig. 12 Transient behaviors of the stored charges at the interfacial nitride of FG and BG side during the erase operation.

4.2 The Optimization of Tunneling Oxide Thickness

Figure 9 and Fig. 10 show the threshold voltage shift of neighboring programmed states for various tunneling oxide thicknesses with a fixed 4.1 eV for the WF_{FG} and 5.2 eV for the WF_{BG}. Figure 9 shows that $V_{T,10}$–$V_{T,01}$ increased as the thickness of the FG tunneling oxide (T_{FG_OX}) decreased. Because a thinner T_{FG_OX} made electrons easier to tunnel through the tunneling oxide, more charges were trapped in the nitride interface. Figure 10 shows that $V_{T,01}$–$V_{T,00}$ decreased and $V_{T,10}$–$V_{T,01}$ increased as the thickness of the BG tunneling oxide (T_{BG_OX}) increased. With the decrement of $V_{T,01}$, $V_{T,01}$ approached $V_{T,10}$; but, it became more distant from $V_{T,00}$. In terms of the threshold voltage shift, 2 nm for T_{FG_OX} and 2 nm for T_{BG_OX} were the optimized tunneling oxide thicknesses. Also, it was found that lowering the workfunction resulted in the same effect of thinning the gate oxide thickness and vice versa.

5. The Transient Characteristics of the Proposed Device

Figure 11 shows the transient behaviors of threshold voltage of the ASDG NVM cell during programming in four different states. A programming bias was selected to perform during the 10 μsec (10^{-5} sec). With T_{FG_OX}=2 nm and T_{BG_OX}=2 nm, a 15 V of programming bias was used to obtain a 10 μsec programming time.

The negative gate with a grounded channel erase (NGCE) method by FN-tunneling was used as an "erase" mechanism [17]. Figure 12 shows the transient behaviors of stored charges at the FG and BG side nitride interfaces during the "erase" operation. The optimized structure achieved from the programming condition was used. Two-bits were erased simultaneously from state "11" to state "00" with −10 V of FG and BG bias and a grounded source/drain. Figure 12 shows that the erasing speed of the FG was faster than that of BG due to the lower workfunction. Due to the fast erasing, FG showed the characteristics of over-erase. However, with a NAND array cell, the over-erase is not a large concern. To erase the stored data in an ASDG NVM within 1 msec, the "erase" voltage was −10 V.

Bit 1 at the FG was erased more rapidly than bit 2 at the BG due to the lower workfunction and thinner tunneling oxide thickness of the FG side. Table 2 shows the threshold voltage differences of the neighboring programmed states for various FG and BG tunneling oxide thicknesses with a 10 μsec programming time. To distinguish state "01" and "10," the case of T_{FG_OX}=2 nm and T_{BG_OX}=2 nm showed the largest threshold voltage difference. Bias conditions are summarized in Table 3 for the read/program/erase operation.

Table 2 The threshold voltage difference of neighboring states with a 10 μsec of the programming time.

Oxide Thickness [nm]	$V_{T,01}$–$V_{T,00}$ [V]	$V_{T,10}$–$V_{T,01}$ [V]	$V_{T,11}$–$V_{T,10}$ [V]
$T_{FG,OX}$= 2 $T_{BG,OX}$= 2	2.04	1.72	3.03
$T_{FG,OX}$= 1 $T_{BG,OX}$= 4	2.44	0.98	3.59
$T_{FG,OX}$= 1 $T_{BG,OX}$= 2	2.82	0.35	4.46

Table 3 The optimized bias condition that gives the 10 μsec programming time and 1 msec erase time.

operation	V_{FG}[V]	V_{BG}[V]	V_{DS}[V]
read	2.7	2.7	0.1
program "01"	0	15	0
program "10"	15	0	0
program "11"	15	15	0
erase	–10	–10	0

6. Conclusions

In this paper, an ASDG NVM was proposed as a breakthrough to the 45-nm barrier. Additionally, it was optimized with various device parameters and read/program/erase operation conditions. To widen the on-current window, an asymmetric double gate with symmetric tunneling oxide thickness was proposed. Finally, WF_{FG} = 4.1 eV, WF_{BG} =5.2 eV, T_{FG_OX} = 2 nm and T_{BG_OX} = 2 nm were adopted as the optimized device parameters. The specific bias and time conditions of the read/program/erase operation to perform the programming operation within 10 μsec and the erasing operation within 1 msec are shown in Table 3. The ASDG NVM can become one of the major candidates of future nonvolatile memory with the characteristics of 2-bit operation using a conventional process.

Acknowledgments

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References

[1] L. Stefan, "Future trends of nonvolatile memory technology," Intel Press Release, 2001.
[2] L. Stenfan, "Non-volatile memories: A look into the future," MIT-Stanford-UC Berkeley Nanotechnology Forum, 2004.
[3] H.I. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nanocrystal memory," IEEE Trans. Electron Devices, vol.43, no.9, pp.1553–1558, 1996.
[4] Y.-C. King, T.-J. King, and C. Hu, "Charge-trap memory device fabricated by oxidation of Si Ge," IEEE Trans. Electron Devices, vol.48, no.4, pp.696–700, 2001.
[5] B. Eitan, R. Kazerounian, A. Roy, G. Crisenza, P. Cappelletti, and A. Modelli, "Multilevel flash cells and their trade-offs," IEEE IEDM Tech. Dig., pp.169–172, 1996.
[6] M.H. White, Y. Yang, A. Purwar, and M.L. French, "A low voltage SONOS nonvolatile semiconductor memory technology," IEEE Trans. Compon. Packag. Manuf. Technol. A, vol.20, no.2, pp.190–195, 1997.
[7] H.C. Wann and C. Hu, "High-endurance ultrathin tunnel oxide in MONOS device structure for dynamic memory application," IEEE Electron. Device Lett., vol.16, pp.491–493, Nov. 1995.
[8] T. Cho, Y.-T. Lee, E.-C. Kim, J.-W. Lee, S. Choi, S. Lee, D.-H. Kim, W.-G. Han, Y.-H. Lim, J.-D. Lee, J.-D. Choi, and K.-D. Seo, "A dual-mode NAND flash memory: 1-Gb multilevel and high-performance 512-Mb single-level modes," International Solid-State Circuits Conference, vol.36, no.11, pp.1700–1706, 2001.
[9] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," IEEE Electron. Device Lett., vol.21, no.11, pp.543–545, 2000.
[10] K.H. Yuen, T.Y. Man, A.C.K. Chan, and M. Chan, "A 2-bit MONOS nonvolatile memory cell based on asymmetric double gate MOSFET structure," IEEE Electron. Device Lett., vol.24, no.8, pp.518–520, 2003.
[11] P. Xuan, M. She, B. Harteneck, A. Liddle, J. Bokor, and T.-J. King, "FinFET SONOS flash memory for embedded applications," IEEE IEDM Tech. Dig., pp.609–612, 2003.
[12] Y.-K. Choi, D. Ha, E. Snow, J. Bokor, and T.-J. King, "Reliability study of CMOS FinFETs," IEEE IEDM Tech. Dig., pp.177–180, 2003.
[13] S.-J. Kim, J.-Y. Kim, S.-B. Yi, S.-B. Lee, and K.-Y. Seo, "Fabrication and characteristic of scaled SONOSFET nonvolatile memory devices for full-featured EEPROMS," Proc. 5th Int. Conf. Properties and Applications of Dielecrtic Materials, vol.2, pp.937–939, 1997.
[14] M.H. White, D.A. Adams, and J. Bu, "On the go with SONOS," IEEE Circuits Devices Mag., vol.16, pp.22–31, 2000.
[15] J. Bu and M.H. White, "Improvement in retention reliability of SONOS nonvolatile memory devices by two-step high temperature deuterium anneals," Proc. 39th Annu. IEEE Int. Reliability Physics Symp., pp.52–56, 2001.
[16] M.H. White, Y. Yang, A. Purwar, and M.L. French, "A low voltage SONOS nonvolatile semiconductor memory technology," IEEE Trans. Compon. Packag. Manuf. Technol. A, vol.20, no.2, pp.190–195, 1997.
[17] N. Kodama, K. Saitoh, H. Shirai, T. Okazawa, and Y. Hokari, "A 5 V only 16 Mbit hash EEPROM cell using highly reliable write/erase technology," Symposium on VLSI Technology Dig. Tech. Papers, pp.75–76, 1991.

Kuk-Hwan Kim received a B.S. in Electrical, Electronic Engineering from Yonsei University in 2005. Since 2005 he is currently pursuing an M.S. degree in the Korea Advanced Institute of Science and Technology. His research interests include nano scale CMOS devices and multi-bit non volatile memory.

Hyunjin Lee was born in Taejon, Korea, in 1979. She received a B.S. and an M.S. degree in electrical engineering from the Korea Advanced Instituted of Science and Technology (KAIST), Taejon, Korea, in 2001 and 2003, respectively. She is currently working toward a Ph.D. Her research interests include reliability issues and nonvolatile memory.

Yang-Kyu Choi received B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1989 and 1991, respectively. He received M.S. and Ph.D. degrees from the University of California at Berkeley in 1999 and 2001, respectively. From January 1991 through July 1997, he worked for Hynix Co., Ltd., Kyungki-Do, Korea, where he developed high-density memory devices. He was a post-doctoral Researcher working on nanobio-technology at the University of California at Berkeley from 2001 to 2003. He is currently an Assistant Professor with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejon. His research interests are novel MOSFET structures such as UTBFET and FinFET, nanofabrication technology for bio-electronics, NEMS, and investigation of quantum phenomena for nanoscale CMOS. He has authored or co-authored over 50 papers, and holds seven U.S. patents and 99 Korean patents. Dr. Choi received the Sakrison Award for the best dissertation in the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in 2002. He also received the Samsung Humantech Thesis Prize in 2000 and a Best Student Paper Award at the International Semiconductor Device Research Symposium in 2001 and at the International SOI Conference. His biographic profile was published in the 57th *Marquis Who's Who in America*.