Silicon photonics-wireless interface ICs for micro-/millimeter-wave fiber-wireless networks

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Abstract: We present two types of Si photonics-wireless interface (PWI) integrated circuits (ICs) realized in standard Si technology. Our PWI ICs convert optical signals into radio-frequency (RF) signals for downlink remote antenna units in fiber-wireless networks. Characterization and modeling of Si avalanche photodetectors (APDs) fabricated in two different Si technologies are carried out and used for PWI IC design. A 5-GHz RF-over-fiber PWI IC composed of APD, preamplifier, and power amplifier (PA) is fabricated in 0.18-μm CMOS technology and its performance is verified by 54-Mb/s wireless local area network data transmission. A 60-GHz baseband-over-fiber PWI IC containing APD, baseband photoreceiver, 60-GHz binary phase-shift keying (BPSK) modulator, and 60-GHz PA is realized in 0.25-μm SiGe BiCMOS technology. Error-free transmission of 1.6-Gb/s BPSK data in 60 GHz with this PWI IC is successfully achieved.

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1. Introduction

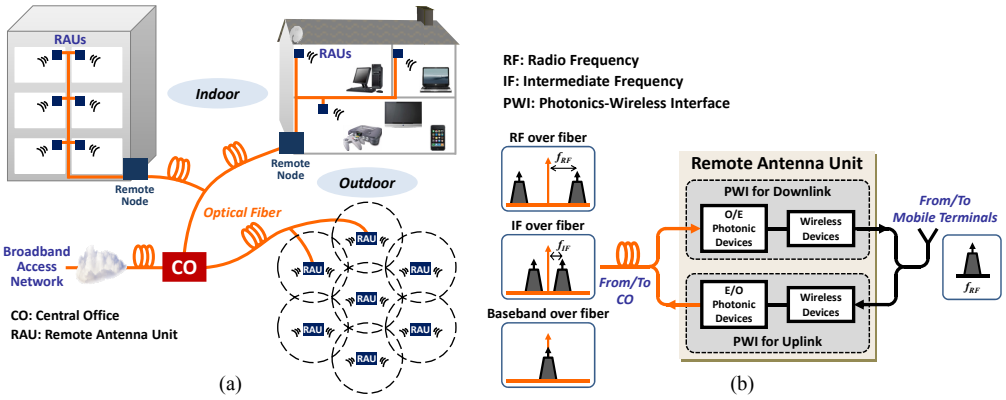

Fig. 1. Schematic block diagrams of (a) fiber-wireless network and (b) three different fiber-wireless network schemes: RF over fiber, IF over fiber, and baseband over fiber.

With the wide spread of various mobile devices that are continuously demanding more data capacity and better accessibility, smart and efficient techniques for linking fiber-based wireline networks with wireless networks are in great demand. Fiber-wireless networks in which fiber is used for linking broadband access networks with remote antenna units (RAUs) located indoor and outdoor for various wireless applications is a promising technology [1–5]. Figure 1(a) shows the schematic block diagram of such fiber-wireless networks. As shown in Fig. 1(b), RAUs provide photonics-wireless interface (PWI) for both downlink and uplink.

The overall system cost of fiber-wireless network is strongly influenced by RAU costs because wireless technologies are increasingly requiring more cells having smaller coverage sizes. One promising solution for realizing cost-effective RAUs is using Si electronic-photonic integrated circuit (EPIC) technology in which both photonic devices and high-speed electronic circuits are integrated on a single Si platform. Si photonics has shown significant performance improvement over the years and high-speed Si modulators [6,7] and Ge photodetectors (PDs) on Si [8,9] have been realized. In addition, Si electronic circuits have become fast enough to cover millimeter-wave and even THz applications [10].

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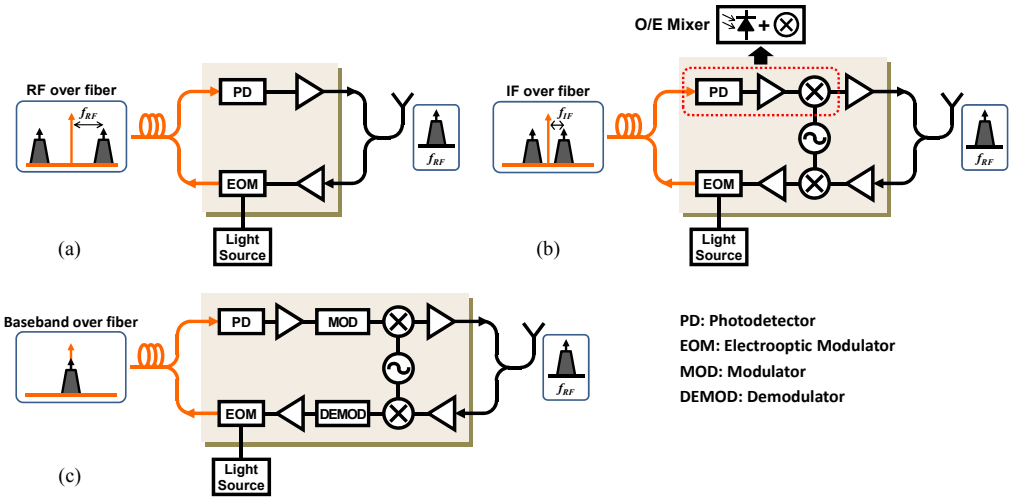

Fig. 2. Block diagrams of Si integrated RAUs for (a) RF-over-fiber, (b) IF-over-fiber, and (c) baseband-over-fiber optical data distribution schemes.

Figure 2 shows block diagrams of RAU architectures that are possible with Si EPIC technology. The RAU architecture depends on whether radio-frequency (RF), intermediate-frequency (IF), or baseband signals are transmitted over fiber. The RF-over-fiber scheme shown in Fig. 2(a) is the simplest because RAU does not have to perform any signal processing except O/E, E/O conversion and amplification. However, the bandwidth of photonic devices should be high enough to handle RF signals, which can be challenging especially for millimeter-wave applications. The IF-over-fiber scheme shown in Fig. 2(b) lessens the bandwidth requirement of photonic devices, but RAU has to perform frequency up-/down-conversion with an electrical frequency synthesizer. The complexity can be reduced with O/E mixers [11], which directly convert optical IF signals into electrical RF signals. The baseband-over-fiber RAU shown in Fig. 2(c) is the most complex because it has to perform data modulation and demodulation as well as up-/down-conversion. But this scheme can offer flexibility in network operation since MAC protocols for optical and wireless networks can be separated [5].

As a feasibility demonstration of Si integrated RAUs, we attempt to realize PWI integrated circuits (ICs) for downlink applications with standard bulk Si technology. Although Si photonics technology can provide Si waveguides with SOI (Silicon-On-Insulator) structures and other photonic devices based on waveguides [12], currently there are no foundry services open to university researchers that support both Si photonics and electronics on a single wafer. Consequently, our investigation is limited to realization of PWI ICs containing Si PDs on bulk Si, which can detect 850-nm light, along with Si electronics for downlink applications.

In this paper, we report two types of PWI ICs realized in standard CMOS and BiCMOS technologies. First, equivalent circuit models for the Si avalanche PDs (APDs) that play a critical role in both of our PWI ICs are developed. The first type PWI IC realized in 0.18-μm CMOS technology detects 5-GHz modulated optical data, performs amplification, and produces 5-GHz wireless signal as is required for RF-over-fiber scheme. The initial simulation results for this PWI IC were reported in [13]. With this PWI IC, successful transmission of 54-Mb/s wireless local area network (WLAN) data is achieved. The second type PWI IC realized in 0.25-μm SiGe:C BiCMOS technology detects and amplifies baseband optical data, performs binary phase-shift keying (BPSK) modulation in 60 GHz, and produces 60-GHz BPSK signal for baseband-over-fiber scheme. Initial measurement results for this PWI IC were reported in [14].

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This paper is organized as follows. Section 2 gives the device characteristics and the equivalent circuit model of Si APD. Section 3 discusses the design, simulation, and WLAN data transmission results of 5-GHz PWI IC. Section 4 gives detailed circuit description and measurement results of 60-GHz PWI IC. Finally, Section 5 concludes this paper.

2. Si APDs

2.1 Device description of Si APD

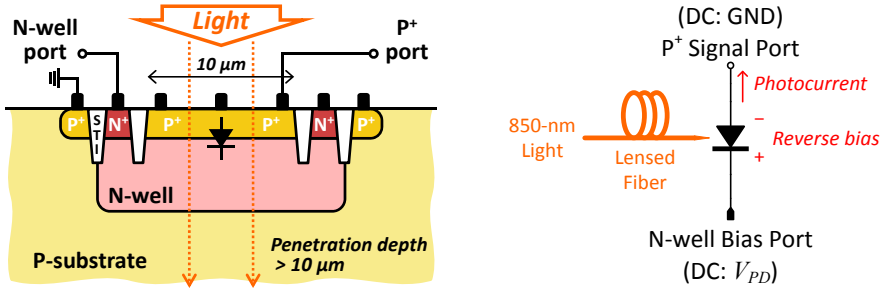

Fig. 3. (a) Cross-section view and (b) port configuration of APD.

Figure 3(a) shows the cross-section view of the APD used in our work. It is realized in standard CMOS or BiCMOS technology without any design rule violation. It is based on P^+/N-well junction so that higher photodetection bandwidth can be achieved without slow diffusive photocurrent in the P-substrate region [15]. Low intrinsic responsivity of the thin P^+/N-well region is enhanced by avalanche multiplication. Undesired photocurrent contribution from P-substrate is prevented by collecting the output current at the P^+ port. Figure 3(b) shows the port configuration used in our PWI ICs.

APDs realized in different technologies have slightly different characteristics due to different doping profiles. The APD realized in 0.18-μm CMOS technology for our 5-GHz PWI IC has the avalanche breakdown voltage of about 10.86 V, maximum DC responsivity of 7.09 A/W with avalanche gain of 548.1 at the incident optical power of −8 dBm. The APD fabricated in 0.25-μm BiCMOS technology used for our 60-GHz PWI IC has breakdown voltage of around 12.52 V, maximum DC responsivity and avalanche gain of 6.43 A/W and 482.0, respectively.

2.2 Modeling for Si APD

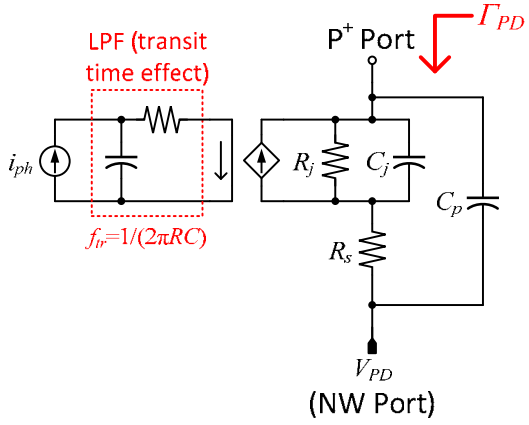

Fig. 4. Small-signal equivalent circuit model of APD.

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APD equivalent circuit models are essential for optimal design of the amplifier stage following the APD. Figure 4 illustrates the APD model used in our work. R_j and C_j represent the junction resistance and capacitance of the P^+/N-well depletion region. R_s represents the N-well resistance from the P^+/N-well junction to the N-well electrodes. C_p is the parasitic capacitance between P^+ and N-well electrodes. The transit time effect is modeled with a current-controlled current source and a first-order RC low-pass filter (LPF). In this work, APDs are biased such that they provide the very minimum avalanche gain necessary. This is because large APD gain reduces the receiver signal-to-noise ratio (SNR) resulting in worse receiver performance [16]. With small APD gain, the avalanche gain process does not strongly influence APD dynamics and we can eliminate the inductive component from the complete APD equivalent circuit model reported in [17] without losing too much accuracy.

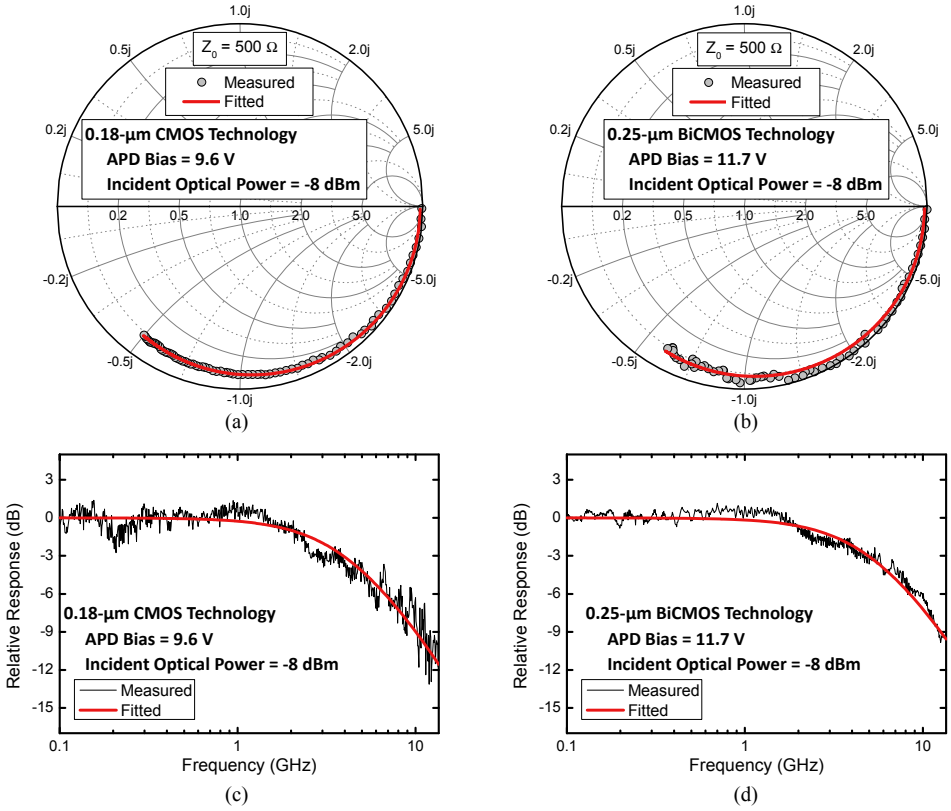

Fig. 5. (a),(b) Measured and fitted results of input impedance on impedance Smith chart normalized by 500 Ω and (c),(d) photodetection frequency responses of APDs realized with CMOS and BiCMOS technologies.

The model parameters are extracted by fitting the simulation results to the measured characteristics at reference V_{PD} of 9.6 V for CMOS APD and 11.7 V for BiCMOS APD. Each V_{PD} is determined for the maximum PWI IC SNR performance. The values for passive components (R_j, C_j, R_s, and C_p) are first extracted from the measured input impedance, Γ_{PD}, characteristics. Figures 5(a) and 5(b) show the measured and fitted Γ_{PD} on the impedance Smith chart normalized by 500 Ω. They do not show any inductive characteristics justifying our omission of the inductive component in the equivalent circuit model. Second, the 3-dB bandwidth is determined from the measured photodetection frequency response. Figures 5(c) and 5(d) show the measured and fitted responses. The APD parameters are listed in Table 1.

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Table 1. APD Parameters

	CMOS APD	BiCMOS APD
Measured Characteristics		
Avalanche breakdown voltage	10.86 V	12.52 V
Maximum DC responsivity	7.09 A/W	6.43 A/W
Maximum DC avalanche gain	548.1	482.0
Photodetection bandwidth	3.92 GHz	4.93 GHz
Model Parameters		
Reference bias voltage	9.6 V	11.7 V
Junction resistance, R_j	70 kΩ	70 kΩ
Junction capacitance, C_j	35 fF	30 fF
Series resistance, R_s	72 Ω	61 Ω
Parasitic capacitance, C_p	13 fF	10 fF
Bandwidth from transit time, f_{tr}	3.98 GHz	5.00 GHz

3. 5-GHz PWI IC in standard CMOS technology

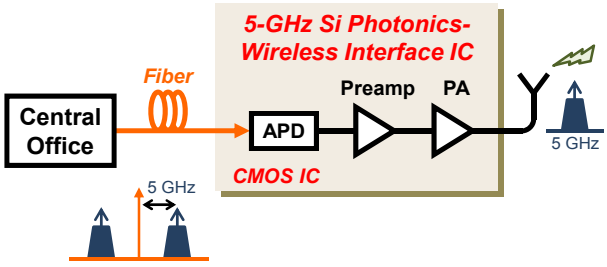

Fig. 6. Block diagram of 5-GHz PWI IC for RF-over-fiber RAU.

Figure 6 shows the block diagram of 5-GHz downlink PWI IC consisting of APD, preamplifier, and power amplifier (PA). Optically transmitted 5-GHz narrowband data in the RF-over-fiber scheme are detected by APD, amplified by preamplifier and PA before radiated into the air with sufficient power. Our PWI IC is optimized for a target application of 54-Mb/s 64 quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) 802.11 5-GHz WLAN data application.

3.1 Circuit description of 5-GHz PWI IC

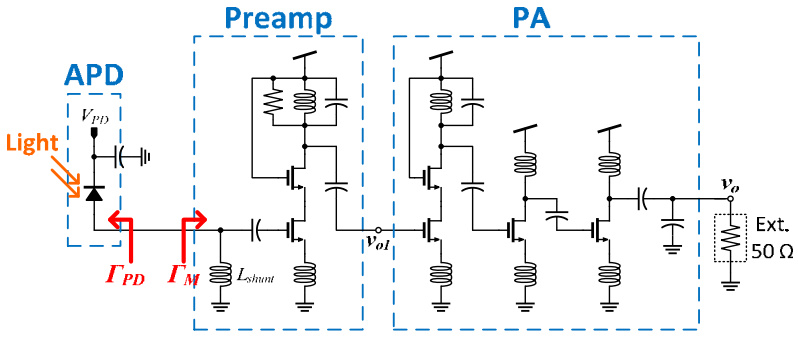

Fig. 7. Schematic of 5-GHz PWI IC.

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Figure 7 shows the schematic of the 5-GHz PWI IC. The overall design is optimized at the operational frequency of 5.4 GHz. An 8-pF bypass on-chip capacitor provides AC ground path at the N-well port of the APD. The preamplifier is a one-stage cascode narrowband amplifier with a source degeneration inductor and a parallel RLC load. Gain and noise performances of the preamplifier are optimized by the impedance matching between APD and preamplifier [18]. L_{shunt} acts as both an impedance matching component and a DC current path for the APD. The PA is a three-stage amplifier designed to provide enough gain and power handling capacity for driving an external 50-Ω load.

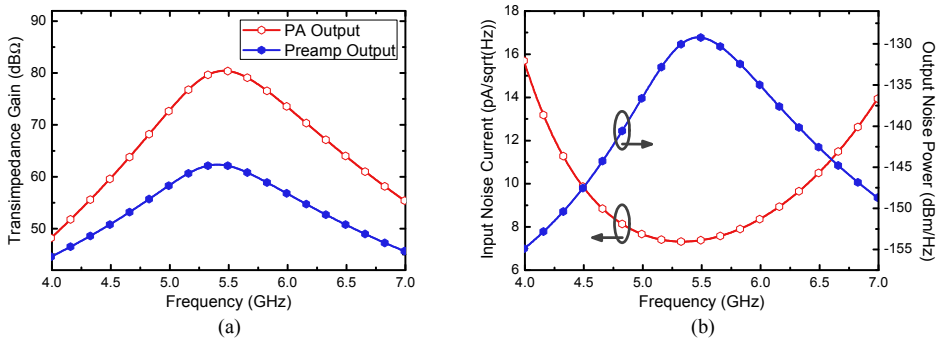

Fig. 8. Simulated (a) transimpedance gain and (b) input and output noise characteristics of 5-GHz PWI IC.

Figure 8(a) shows the simulated transimpedance gain at preamplifier output, v_{o1}, and PA output, v_o. The preamplifier peak gain is 62.3 dBΩ at 5.4 GHz and the overall gain is 80.4 dBΩ after the PA with a 50-Ω load. The 3-dB bandwidth is 0.6 GHz from 5.18 to 5.78 GHz. Figure 8(b) shows the simulated input-referred noise current and output noise spectrum. Noise simulation takes into account only the circuit noise. The minimum input noise current is 7.32 pA/√Hz at 5.35 GHz and, within 3-dB bandwidth, it is less than 7.8 pA/√Hz. The peak output noise power is −129.2 dBm/Hz at 5.47 GHz.

3.2 5-GHz RF-over-fiber wireless downlink demonstration

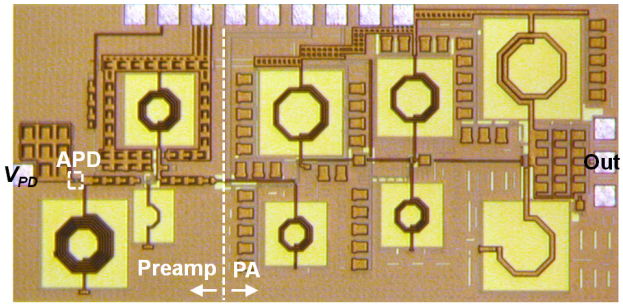

Fig. 9. Chip photo of 5-GHz PWI IC.

Figure 9 shows the chip photo of the 5-GHz PWI IC. The chip area including all probe pads is 0.9 mm × 1.8 mm. The IC consumes 155.7 mW from 1.8-V supply. The PA consumes most of the power.

Figure 10 shows the experimental setup used for RF-over-fiber demonstration. A vector signal generator provides 54-Mb/s WLAN data in 5 GHz. An 850-nm electrooptic modulator (EOM) modulates light from an 850-nm laser diode with the WLAN signals. Modulating electrical power is set to −21 dBm in order to minimize the EOM nonlinearity. The optical signal is injected through a lensed fiber into the PWI IC in an on-wafer probing setup. The PWI IC converts the optical signal into the wireless signal whose spectrum is shown in the

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inset of Fig. 10. The output signal is down-converted and its error vector magnitude (EVM) performance is evaluated by the WLAN receiver consisting of a mixer, a frequency synthesizer, an amplifier, and a vector signal analyzer.

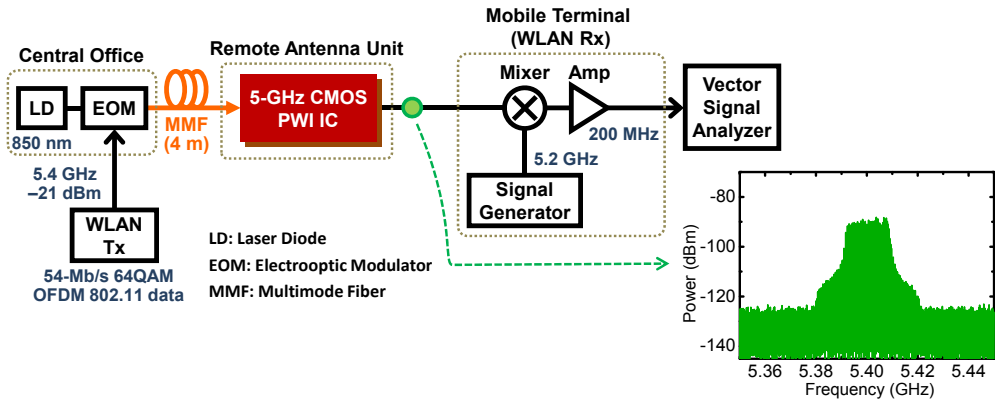

Fig. 10. Demonstration setup for 54-Mb/s WLAN data transmission using 5-GHz PWI IC.

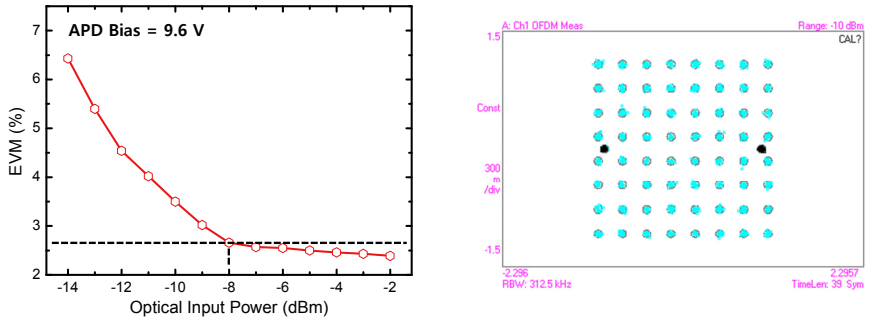

Fig. 11. (a) EVM at different optical input powers and (b) constellation of demodulated data at optical input power of −8 dBm.

Figure 11(a) shows the EVM at different optical input powers. At low powers, the link performance degrades as optical input power decreases due to reduction in SNR of PWI IC output power. Improvement in EVM and SNR with increasing optical input power saturates at about −8 dBm due to receiver nonlinearity. Figure 11(b) shows the constellation of demodulated data at the WLAN receiver at the condition of −8-dBm optical input power.

4. 60-GHz PWI IC in standard BiCMOS technology

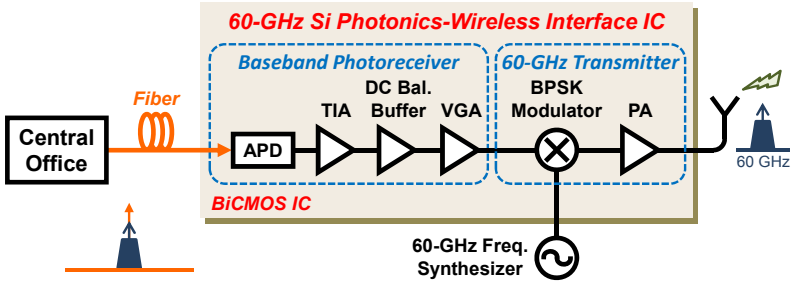

Fig. 12. Block diagram of 60-GHz PWI IC for baseband-over-fiber RAU.

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Figure 12 shows the block diagram of 60-GHz PWI IC realized for baseband-over-fiber applications. The PWI IC is divided into two parts, a baseband photoreceiver and a 60-GHz transmitter. The baseband photoreceiver is composed of APD, transimpedance amplifier (TIA), DC-balanced buffer, and variable-gain amplifier (VGA). The 60-GHz transmitter consists of 60-GHz BPSK modulator and 60-GHz PA. The entire circuit is integrated on a single substrate with IHP's 0.25-μm SiGe:C BiCMOS SG25H3 technology [19].

4.1 Circuit description of 60-GHz PWI IC

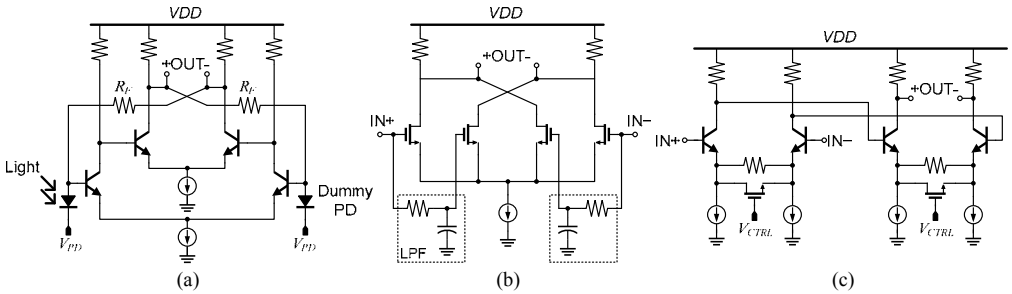

Fig. 13. Schematics of (a) TIA, (b) DC-balanced buffer, and (c) VGA in 60-GHz PWI IC.

Figure 13(a) shows the schematics of TIA, which is a two-stage common-source shunt-feedback differential amplifier. Even though input light is single-ended, a dummy APD is used for symmetry. Figure 13(b) shows the DC-balanced buffer composed of a f_T-doubler amplifier and an LPF having the cut-off frequency of 1 MHz. This buffer converts pseudo-differential TIA output into fully differential. Figure 13(c) shows the schematic of the VGA [20]. The gain is varied by changing on-resistance of the MOS emitter-degeneration variable resistors with the gain control voltage V_{CTRL}.

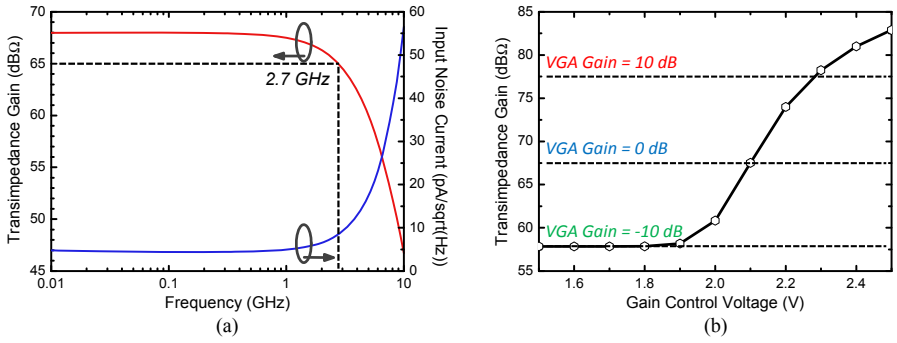

Fig. 14. Simulated (a) transimpedance gain and input noise current of TIA with DC-balanced buffer and (b) total transimpedance gain of baseband photoreceiver at VGA output.

Figure 14(a) shows the simulated TIA transimpedance gain and input-referred noise current with the DC-balanced buffer. The low-frequency gain is about 68 dBΩ and the 3-dB photodetection bandwidth is about 2.7 GHz. The low-frequency input noise current is 4.5 pA/√Hz and, within the signal bandwidth of 2.7 GHz, it is 0.317 μA_{rms}. Figure 14(b) shows the simulated low-frequency transimpedance gain of the baseband photoreceiver measured at the VGA output as a function of the gain control voltage. The gain range is 20 dB from −10 to 10 dB as the gain control voltage varies from 1.9 to 2.3 V.

The millimeter-wave transmitter is composed of 60-GHz BPSK modulator and PA. Figure 15(a) shows the schematic of 60-GHz BPSK modulator, which has a double-balanced Gilbert-cell structure with 60-GHz differential local-oscillator (LO) input. A balun is used as a load inductor to convert differential modulator output signals into single-ended for PA input. Figure 15(b) shows the schematic of 60-GHz PA which is a one-stage single-ended

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cascode amplifier. It has an emitter-degeneration inductor to ensure stable operation. The PA output impedance is optimized for maximum power delivery to 50-Ω external load.

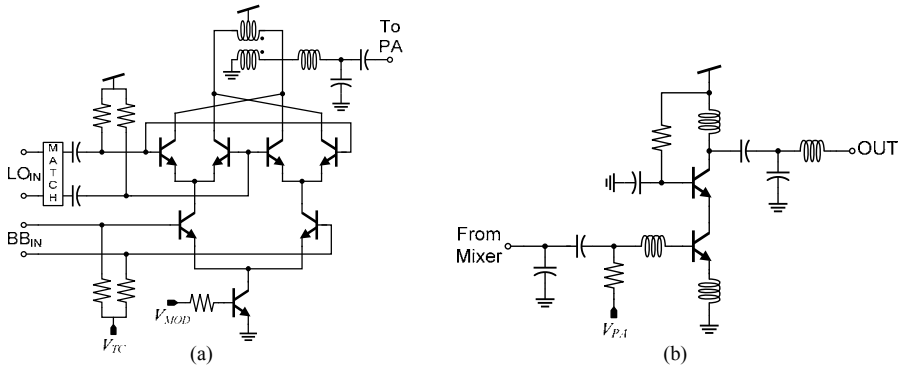

Fig. 15. Schematics of (a) BPSK modulator and (b) PA in 60-GHz PWI IC.

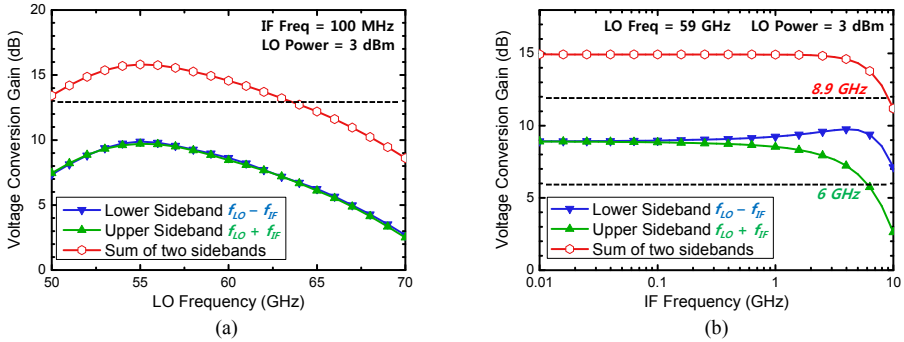

Fig. 16. Simulated voltage conversion gain of 60-GHz transmitter at different (a) LO frequencies and (b) IF frequencies.

Figure 16(a) shows simulated voltage conversion gain of 60-GHz transmitter at different LO frequencies with 100-MHz IF and 3-dBm LO. Since the BPSK modulator is a double-sideband modulator, conversion gains for lower-sideband $f_{LO} - f_{IF}$, upper-sideband $f_{LO} + f_{IF}$, and sum of these two are shown. The peak gain for the sum is about 15.8 dB at 55 GHz. The 3-dB bandwidth is over 14 GHz from 50 to 64 GHz. Figure 16(b) shows voltage conversion gain at different IF frequencies with 3-dBm 59-GHz LO. Responses of two sidebands are not symmetric and the upper-sideband response has lower 3-dB bandwidth of 6 GHz. The combined bandwidth of both sidebands is about 8.9 GHz. This indicates that the IF bandwidth is limited by the baseband photoreceiver, not by the 60-GHz transmitter.

4.2 60-GHz baseband-over-fiber wireless downlink demonstration

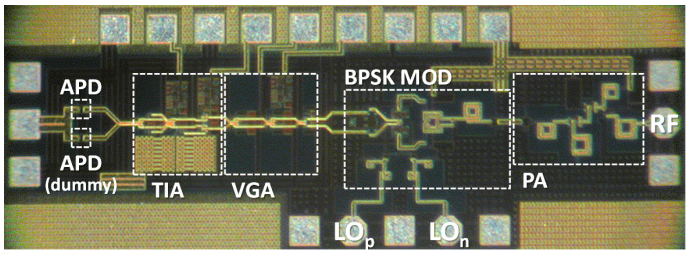

Fig. 17. Chip photo of 60-GHz PWI IC.

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Figure 17 shows the chip photo of 60-GHz PWI IC. The fabricated chip is characterized in an on-wafer probing setup. The chip area including probe pads is 0.5 mm × 1.42 mm. Total power consumption is 163.3 mW, where the baseband photoreceiver consumes 51.4 mW at 2.5-V supply and the 60-GHz transmitter consumes 111.9 mW at 3-V supply.

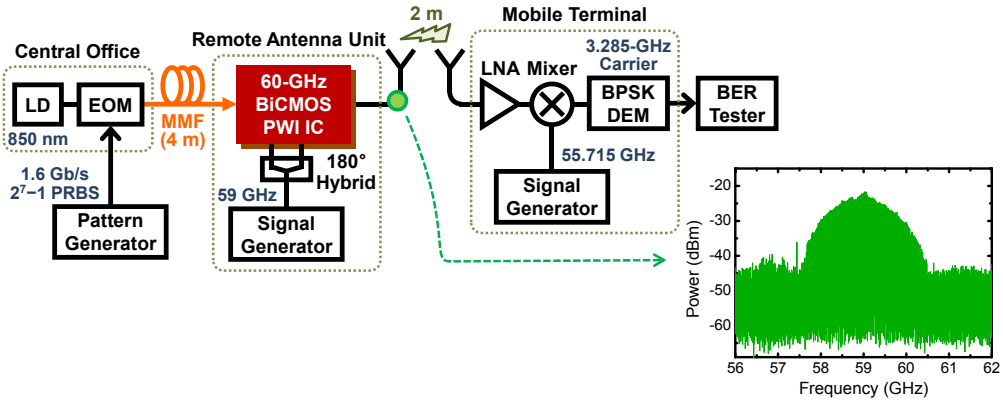

Fig. 18. Demonstration setup for 1.6-Gb/s BPSK data transmission using 60-GHz PWI IC.

The measurement setup shown in Fig. 18 is used for 1.6-Gb/s BPSK data transmission in 60-GHz fiber-wireless downlink with the fabricated PWI IC. In the central office, 850-nm light is modulated with 1.6-Gb/s 2^7-1 pseudo-random binary sequence data and delivered to the PWI IC through 4-m multimode fiber. The PWI IC converts optical signals into 60-GHz BPSK signals with 59-GHz carrier externally provided. The resulting spectrum is shown in the inset of Fig. 18. BPSK data are transmitted to the mobile terminal via 2-m wireless channel, down-converted, demodulated with a custom-designed BPSK demodulator [21], and analyzed by a bit-error rate (BER) tester.

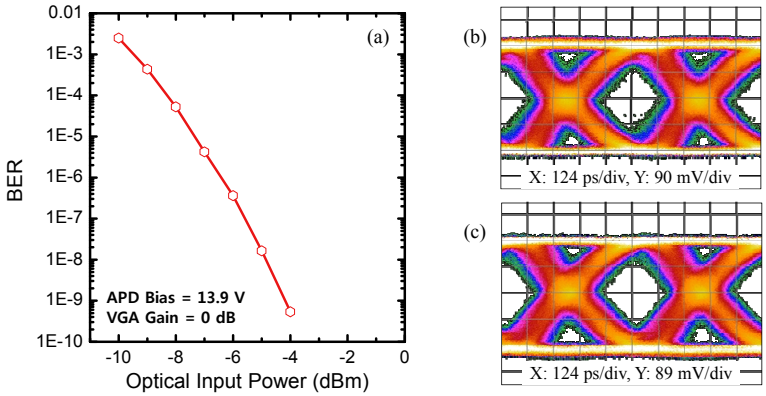

Fig. 19. Measured (a) BER at different optical input powers and eye diagrams of demodulated data at optical input powers of (b) –6 and (c) –3 dBm.

Figure 19(a) shows measured BER at different optical input powers. The lowest BER measured with our 60-GHz PWI IC was 5.36×10^{-10} at –4-dBm optical input power. For the optical input powers of –3, –2, –1, and 0 dBm, our PWI IC did not produce any errors at least for 10^{11} pseudo random bits, which correspond to measuring time of 62.5 seconds with 1.6-Gb/s data rate. Eye diagrams of demodulated data at the optical powers of –6 and –3 dBm are shown in Figs. 19(b) and 19(c). The eye diagram shows very thick transition lines due to intrinsic timing errors in our demodulator [21].

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5. Conclusion

A 5-GHz RF-over-fiber PWI IC and a 60-GHz baseband-over-fiber PWI IC are successfully realized in standard Si technology. The performance of each PWI IC is verified with data transmission in fiber-wireless downlink. Although these PWI ICs have limited functionalities to be used in applications, they demonstrate the feasibility of applying Si EPIC technology for realizing cost-effective and compact RAUs in future fiber-wireless networks.

Acknowledgments

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