Integrated plasmon and dielectric waveguides

Michael Hochberg, Tom Baehr-Jones, Chris Walker & Axel Scherer

California Institute of Technology, Moore Building, 1200 East California Street, Pasadena, CA 91125
Hochberg@caltech.edu

Abstract: We have designed, fabricated and characterized surface plasmon waveguides for near infrared light in the telecommunications spectrum. These waveguides exhibit losses of -1.2dB/μm and can guide light around 0.5 μm bends. Light can also be efficiently coupled between more conventional silicon waveguides and these plasmon waveguides with compact couplers, and we demonstrate that surface plasmon optical devices can be constructed by using planar circuit fabrication techniques. The large optical field enhancements of metallic surface plasmon devices are expected to lead to a new class of plasmonic optical devices, which will take advantage of the large field enhancements at the surfaces of the plasmon waveguides for nonlinear or sensing functionality, while utilizing the low losses available in silicon waveguides to move light longer distances on chip.

OCIS Codes: (130.3120) Integrated optics devices, (130.2790) Guided waves, (240.6680) Surface plasmons.

References and links

1. J. Takahara, Y. Suguru, T. Hiroaki, A. Morimoto, and T. Kobayashi, "Guiding of a one-dimensional optical beam with nanometer diameter," Opt. Lett **22**, 475-477 (1997).
2. W. L. Barnes, A. Dereux, and T. W. Ebbesen, "Surface Plasmon Subwavelength Optics," Nature **424**, 824 - 830 (2003).
3. Palik, E., *Handbook of Optical Constants of Solids* (Academic Press, Washington, D.C., 1985).
4. T. Nikolajsen, K. Leosson, I. Salakhutdinov, and S. Bozhevolnyi, "Polymer-based surface-plasmon-polariton stripe waveguides at telecommunication wavelengths," Appl. Phys. Lett. ***82***, 668-670 (2003).
5. S. A. Maier, P. G. Kik, H. A. Atwater, S. Meltzer, E. Harel, E. E. Koel, and A. A. Requicha, "Local detection of electromagnetic energy transport below the diffraction limit in metal nanoparticle plasmon waveguides," Nature Mat. **2**, 229-232 (2003).
6. P. Berini, "Plasmon-polariton waves guided by thin lossy metal films of finite width: Bound modes of symmetric structures," Phys. Rev. B **61,** 10484-10503 (2000).
7. T. Baehr-Jones, M. Hochberg, C. Walker and A. Scherer, "High-Q ring resonators in thin silicon-on-insulator," Appl. Phys. Lett. **85**, (2004).
8. D. Taillaert, W. Bogaerts, P. Bienstman, T. F. Krauss, P. Van Daele, S. I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, "An Out-of-Plane Grating Coupler for Efficient Butt-Coupling Between Compact Planar Waveguides and Single-Mode Fibers," IEEE J. Quantum Electron. **38**, 949 (2002).
9. V. Almeida, R. Panepucci, and M. Lipson "Nanotaper for compact mode conversion," Opt. Lett. ***28***, 1302-1304 (2003).
10. T. Baehr-Jones, M. Hochberg, and A. Scherer, "A Distributed Implementation of the Finite-Difference Time Domain (FDTD) Method," Applied Computational Electromagnetics Society, 2001.
11. J. Vuckovic, M. Loncar, and A. Scherer, "Surface plasmon enhanced light-emitting diode," IEEE J. Quantum Electron. **36**, 1131-1144 (2000).
12. A. Taflove, *Computational Electromagnetics*, (Artech House, Boston, 1995).
13. W. Henschel, Y. M. Geirgiev, and H. Kurz, "Study of a high contrast process for hydrogen slisesquioxane as a negative tone electron beam resist," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures **21**, 2018-2025 (2003).
14. I. W. Rangelow, and H. Loschner, "Reactive ion etching for microelectrical mechanical system fabrication," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures **13**, 2394-2399 (1995).

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1. Introduction

Future integrated photonic circuits for telecommunications and optical logic applications will require a high level of complexity. Plasmon waveguides, which are constructed out of metal, can be used to guide light in volumes far beneath the diffraction limit [1], offering a possible avenue towards dramatically increased device densities in integrated photonic circuits. Compact plasmon waveguides generally suffer from high loss, and chip-scale integration presents a challenge, as does efficient coupling off-chip [2]. Here we present a material platform in which both plasmon waveguides and dielectric waveguides can be closely integrated. We demonstrate efficient, broadband light transmission between a silicon waveguide and a plasmon waveguide, achieving 3.4 dB of insertion loss, using standard processing tools that are widely available in the semiconductor industry. Our results suggest a material system in which both plasmon and dielectric waveguides can be used together in practical integrated optical circuits.

2. Design

The electromagnetic response of metals in the infrared and visible spectrum is characterized by a largely imaginary index of refraction [3] enabling the definition of waveguides with sub-diffraction scale optical propagation. There is a basic trade-off in all plasmon waveguide geometries between mode size and propagation loss. One can have a low propagation loss at the expense of a large mode size, such as in the work of Nikolajsen et al, who report propagation losses of 6 dB/cm for 20nm slabs of gold, but with a 12 μm mode diameter [4]. At the other extreme, Takahara et al have predicted guiding in 20 nm diameter silver nanowires, with a mode field diameter of about 10 nm, but with theoretical propagation losses of 3 dB/410 nm [1]. Though this loss is acceptable for nano-scale photonic circuitry, large scale integration with such losses is not feasible. While efficient end-fire coupling from fiber modes to large scale plasmon waveguides has been demonstrated [4], a realistic path to large scale integration and off-chip coupling for nano-scale plasmon geometries has to our knowledge not yet been demonstrated. As a result, many of the current measurements that have been made for sub-diffraction scale plasmon optics have been done with direct interrogation methods, such as on-chip fluorescence [5]. Significant work on the modes of plasmon waveguides of small width and thickness has been performed by Berini [6], who showed that at any metal-dielectric interface there will exist a plasmon mode and examined the properties of thin-strip metal waveguides.

Plasmon based-waveguides are not the only way by which light can be guided on small scales. In particular, we have previously demonstrated dielectric ridge waveguides of Silicon in Silicon-On-Insulator (SOI), which have low propagation loss of 6-7 dB/cm [7]. Though the mode size is fundamentally diffraction limited, 90% of the optical energy is contained in a 1.5 square micron region, in such waveguides as we detail below. Due to the low loss achievable, SOI waveguides are a promising path for chip-scale device integration. Perhaps as importantly, numerous geometries for the efficient, broadband coupling from an external fiber to an SOI waveguide have been demonstrated [8,9]. Our goal in this work is therefore to build a system in which both SOI waveguides and nano-scale plasmon waveguides coexist.

Three-dimensional Finite-Difference Time Domain (FDTD) models on a distributed cluster of 45 personal computers [10] were used to design plasmon waveguides by implementing the Drude model to simulate the interaction of the optical field with the metal [11]. A spatial discretization of 10 nm was used, with a time discretization 90% of the stability limit [12]. The modes of a plasmon waveguide formed on the edge of a 100 nm thick layer of silver were solved by spatial filtering, and the waveguide loss was predicted to be roughly -0.4dB/μm for wavelengths between 1.4 and 1.6μm. The silver slab was located on top of a silicon dioxide layer of 1.4 μm thickness, which was in turn supported by a silicon handle. 90% of its optical energy of the plasmon mode is contained in a region of about 1 square micron region at the edge of the silver slab. The entire geometry is clad in polymethylmethacrylate (PMMA), which is known to exhibit low optical losses in the near

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infrared regime [5]. The properties of silicon waveguides formed by a .5 μm ridge waveguide with .12 μm thickness in such a system were also studied. Figure 1 shows simulation results for both modes. Both modes are primarily polarized with the E field parallel to the chip surface.

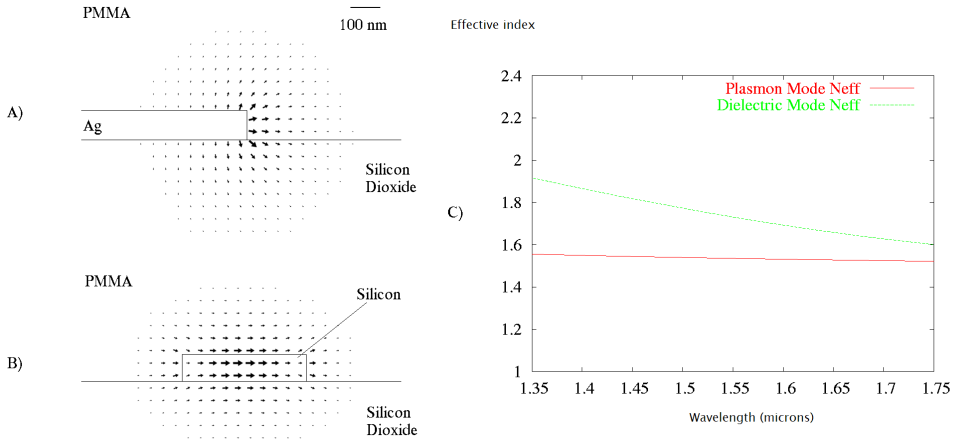

Fig. 1. In A) and B) the E field vector components are rendered for the plasmon and silicon waveguides used in our study. C) shows the dispersion diagrams of both modes.

3. Experiment

To construct optical circuits, SOI wafers were obtained with an approximately 120nm thick top silicon layer and a 1.4 micron buried oxide layer. Dow Corning's HSQ resist [13] was spun onto the chip, baked at 170 C, and silicon waveguides were exposed at 100kV in a commercial electron beam lithography system at 3500 μC/cm^2. After development, pattern transfer was performed using a chlorine ICP plasma [14]. For the metal layer, PMMA resist was again spun onto the surface of the chip, and 100 nm of silver was evaporated followed by a metal liftoff. Finally, a thick layer of PMMA was spun onto the completed sample and baked – this layer served both as a water diffusion barrier in order to protect the silver from oxidizing and as a cladding layer for the waveguides.

Efficient coupling between plasmon and SOI waveguides was achieved by directional coupling. FDTD simulations predicted that a coupling length of 1.8 μm with a 150 nm separation between the plasmon and silicon waveguides resulted in broadband coupling efficiencies with a peak value of 2.4 dB at 1520 nm. In our simulations, it was found that the amount of light coupled between the silicon and metal waveguides oscillated as a function of the length over which they ran parallel to one another, which justifies our characterization of the coupling as directional in nature, as opposed to butt coupling. Figure 2 shows the insertion loss as a function of wavelength, as well as a rendered image of the coupling simulation. Unfortunately, the coupling efficiency suffers greatly from small perturbations in the spacing between the silicon and plasmon waveguides, with FDTD predicted falloffs on the order of 3 dB for 50 nm of offset. The misaligned efficiencies are also plotted in Fig. 2. Because of the high sensitivity to edge misalignment, our multi-layer fabrication had to be performed with a zebra mask by using repeated devices with intentional misalignments of ±50 nm in both Cartesian axes.

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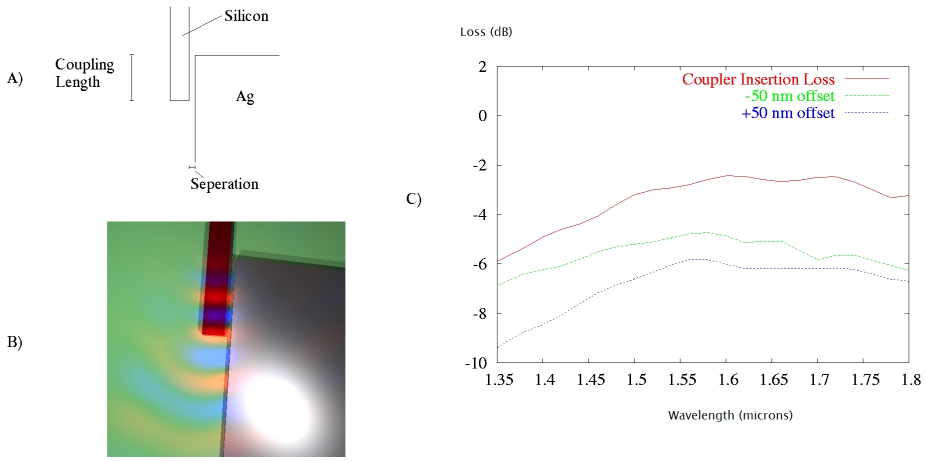

Fig. 2. (a) shows a diagram of the layout of the dielectric plasmon coupling device. A rendering of a simulation is shown in (b), while (c) shows the simulated insertion loss for the coupling device in dB vs wavelength in μm. Also shown are the insertion losses when the coupling device separation is increased or decreased by 50 nm, as might happen due to misalignment in fabrication.

The first type of device that we fabricated consisted of straight plasmon waveguide lengths of varying plasmon propagation lengths, ranging from 2 to 12 μm. An automated, computer controlled optical alignment system was developed for this testing. Light was coupled into and out of the SOI waveguides from a polarization maintaining fiber array employing standard coupling geometries [8]. An input laser was swept in wavelength at -3 dBm laser power to characterize each device, in increments of 0.01 nm. We were able to effectively measure the device responses for free-space wavelengths from 1.5 to 1.53 μm, a bandwidth range that nearly encompasses a fiber-optic teleecommunications band. Baseline calibration loops, which consisted of simple SOI waveguide loops with no plasmon devices, were used to measure the base insertion loss of the test setup and fiber to SOI waveguide coupler performance.

As predicted, the frequency response of our devices was fairly flat in the 1.5-1.53 μm regime. Taking the peak transmission in the 1.51 μm to 1.52 μm spectral region for the best 5 devices of about 150 devices fabricated for each length, we performed a linear regression to identify the coupling insertion loss, and propagation loss of the plasmon waveguide. These values were found to be 4.2±1.6 dB and 1.3±.4 dB/μm respectively. The best device measured demonstrated 3.4±.4 dB of coupling insertion loss. The coupling efficiency measured is in agreement with the predicted value from FDTD, while the propagation loss is clearly higher in the plasmon waveguide; this is most likely a result of fabricated imperfections in the silver slab edge. The fitted line, and a scatter plot of this data are shown in Fig. 3. The error scatter in the data is not quite Gaussian, likely due to our use of a zebra mask strategy to deal with misalignments between the lithography layers.

There is substantial coupling between the silicon waveguides in the absence of any metal structure. Because of the high absorption of the plasmon waveguides, the loss from free space coupling is similar to the losses from the plasmon waveguides, and thus a comparison of straight waveguide devices with and without metal structures does not provide compelling evidence of plasmon guiding. Our simulations, however, show that the free space mode is completely disrupted by the addition of the metal structure. Furthermore, with the addition of 1 um x 1um defects sticking out of the metal (similar to those shown below for the bend devices), the plasmon mode is completely disrupted. The extinction measurements with these

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defects added were limited by the noise floor on the measurement setup, giving an overall extinction consistently in excess of 10 dB between devices with the defect and those without. Because of the high degree of localization of the defect, it would not be expected to greatly attenuate free space coupling. However, such defects were found in simulations to completely disrupt the transmission of the plasmon mode. Because of the good coupling in the absence of the metal, these structures do not provide compelling evidence for plasmon guiding, but with the bend data below to confirm the guiding and the coupling, can be legitimately used to characterize the waveguide losses.

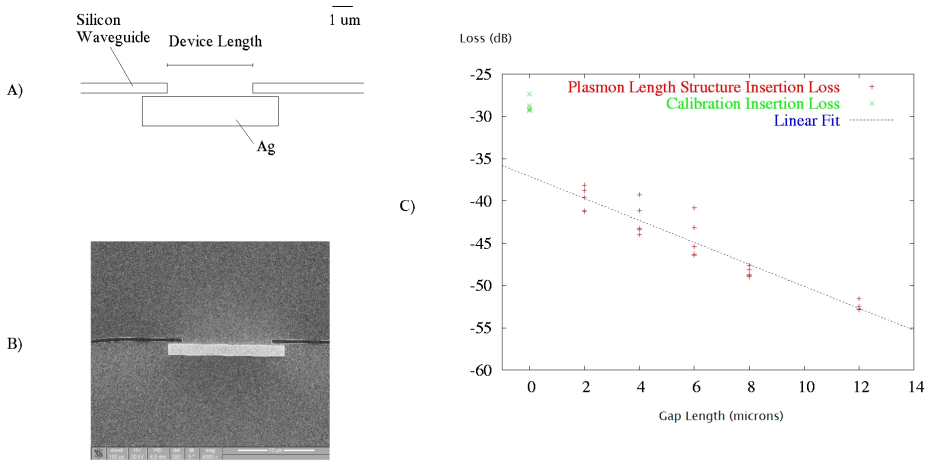

Fig. 3. (a) shows a diagram of the layout of a plasmon waveguide length device, and (b) shows an SEM image of a fabricated device. (c) shows the scatter plot and fitted line, as well as a scatter plot of the 5 best calibration insertion loss structures for contrast. The axes are fiber to fiber insertion loss in dB versus plasmon waveguide length in μm.

Naturally, we wished to confirm that plasmon guiding was actually occurring, as opposed to free space coupling between the silicon waveguides. Curved plasmon waveguide devices were fabricated, which utilize tight plasmon waveguiding to achieve small bend radii. These devices were fabricated with the plasmon-dielectric couplers detailed above, and with bend radii of 0.5 μm. In Fig. 4, we show the plasmon bend device, a plasmon bend device with a defect added, and a device with no metal layer. We also show renderings of the FDTD simulations, as well as the simulation results. Finally, we show the measured data from fabricated devices. We have chosen the best device measurements, selected from about 25 devices of each type. For transparency, we show the raw data measured, as well as the test setup baseline curve, which is the fiber to fiber insertion loss for a simple SOI waveguide calibration loop. The ripple observed in the spectra is due to return losses on chip and on our input couplers forming cavities. FDTD simulations predict that the 0.5 μm bend device should have 11 dB of insertion loss in the 1.5-1.53 μm range, while the defect introduces 16 dB of loss for the entire bend. Perhaps more importantly, a complete absence of a metal layer induces an insertion loss of 25 dB. The measured device performance is in approximate agreement with these values, when the testing noise floor of -55 dB is taken into account. Note that the nearly 15 dB extinction observed in the bend calibration device is closer to the simulated value of 11 dB, since the propagation loss of the plasmon waveguide is about .9 dB/μm above the simulated value, most likely due to edge roughness.

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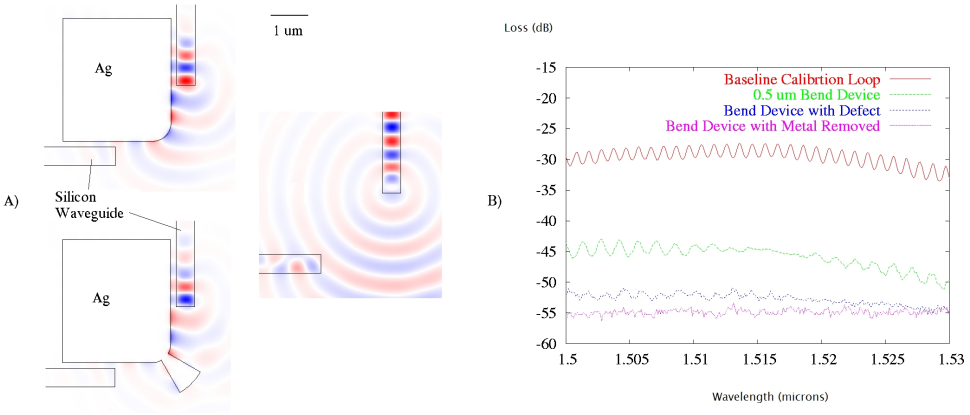

Fig. 4. Device layouts and renderings from FDTD simulations are shown in A), for the non-defective, metal-free, and defective devices, clockwise from top left. The out-of plane H field is rendered as blue and red. In B), the transmission spectra of the best measured devices of each type are shown, with fiber to fiber insertion loss in dB plotted against laser wavelength in μm. The baseline calibration loop spectrum is also shown for comparison.

4. Conclusion

To summarize, we have demonstrated a viable material platform for the construction of integrated dielectric-plasmon circuits. We emphasize that our planar process uses SOI wafers that are commercially available. When our plasmon-dielectric coupling efficiencies of 2.4 dB are combined with the fiber to dielectric insertion losses of 7.7 dB achieved in waveguiding geometries similar to ours [7], we believe that this provides a technological path for the coupling of radiation from an optical fiber to a nano-scale plasmon waveguide, and an important step in the realization of practical plasmon optical devices.

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