ECS Journal of Solid State Science and Technology, **8** (7) Q3195-Q3201 (2019)

JSS FOCUS ISSUE ON GALLIUM OXIDE BASED MATERIALS AND DEVICES

Thermal Simulations of High Current β-Ga_2O_3 Schottky Rectifiers

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The temperature rise and distribution in large area β-Ga_2O_3 rectifiers is simulated using self-consistent solution of the partial differential equations governing the physics in the electrical and thermal domains with the Florida Object Oriented Device and Process simulator (FLOODS) TCAD simulator. The effect of forward voltage (0−2.5V) and power (0−5.5W) was examined for the different epitaxial layer and bulk substrate thicknesses, as well as edge termination and heat sink geometry. A higher maximum temperature is seen for the devices with thicker bulk substrates, while the effect of Joule heating was more evident in the thinner epi-layer structures since the resistance decreases and the power generation increases, resulting in a higher temperature. The maximum temperature rise was ∼170K under high power conditions. The heat sink simulation results show a drop in the maximum temperature, where a Cu fin heat sink reduced the maximum temperature by 26.76%.
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Manuscript submitted January 14, 2019; revised manuscript received March 1, 2019. Published March 29, 2019. *This paper is part of the JSS Focus Issue on Gallium Oxide Based Materials and Devices.*

Gallium oxide has recently gained a lot of interest for its potential in power electronics applications because it has a larger bandgap compared to other wide bandgap (WBG) materials like 4H-Silicon carbide (SiC) and gallium nitride (GaN). Power switching applications require high electric breakdown strength, low on-resistance and low charge storage times.[1–3] Many recent review articles on Ga_2O_3 focus on the large bandgap (∼4.8eV), high power applications, n-type doping controllability during bulk or epitaxial growth using Si or Sn dopants and ease of manufacturing for large, high quality wafers, with β-Ga_2O_3 being the most stable polymorph under normal conditions.[4–7] Furthermore, there has also been some focus on the applications of Ga_2O_3 as high temperature gas sensing, photo-catalysts, truly solar-blind photodetectors, phosphors, and optoelectronic devices.[8,9,1] It also has a larger potential figure-of-merit (FOM) than GaN and SiC (Table I), which is used to evaluate the suitability of semiconductors for electronic power switches. For Ga_2O_3, large bandgap translates into a high critical field strength of 7–8 MV/cm, which is reflected in a high Baliga's figure-of-merit (BFOM). The BFOM for Ga_2O_3 is about 4–7 times higher than that for SiC, hence leads to low conductance losses at a lower cost in comparison to 4H-SiC diodes.[10]

The thermal conductivity for Ga_2O_3 is an order of magnitude lower than that for its commercial counterparts, i.e. SiC and GaN (Table I) which means modeling the heat dissipation in and from the β-Ga_2O_3 devices requires more research. In addition to SiC and GaN, the high Al AlGaN alloys also provide promise, but high contact resistance remains an issue. Furthermore, lack of large area and cheap native substrates and issues with vertical conductivity may limit its use in vertical power devices.[11–14] The thermal conductivity of Ga_2O_3 is about 10–20 times lower than that of 4H-SiC depending on the crystallographic direction, which reflects the difficulty in incorporating this material as a commercial option for ultra-high power density applications. This can be explained by the self-heating effects (Joule heating) and the lack of efficient heat dissipation through the material, compared to other WBG materials.

Some recent studies done on Ga_2O_3 Schottky diode rectifiers reported impressive electrical performance, which is due to the rapid progress in epitaxial growth methods. The impressive performance includes a forward current density of 421 A/cm^2 and R_{on} of 2.9mΩ.cm^2,[15] and specific on-resistance of 5.1 mΩ.cm^2.[16] In our study, we focus on the forward current-voltage (I-V) characteristics,[17–19] achieving a high forward current of 1–2 Amps for different device sizes and doping profiles. These studies focus on the realization of the large dimension devices with a very high forward current, and high breakdown voltages, hence it is important to understand the trends in self-heating and how they affect device performance which is done via a comprehensive simulation study.

Most of the power generated is going to dissipate through the channel and this will cause an increase in temperature within the channel. The rise in the channel temperature will cause an increase in the electron-phonon scattering, which would result in degradation of the electron transport properties (electron mobility), eventually causing a loss in the device performance. Hence, it is important to understand this rise in temperature and develop successful heat dissipation mechanisms either through cooling fans or heat sinks.

Simulation Methods

The partial differential equations governing the physics in the electrical and thermal domains are solved self-consistently with the FLOODS TCAD simulator. The Florida Object Oriented Device and Process Simulator (FLOODS/FLOOPS) is a partial differential equation (PDE) solver, written as an extension to the Tcl language for easy specification of PDEs and boundary conditions.[20] The non-linear equations that are solved within it are done so by the Newton method and they are discretized in space using the finite element method. We apply a two-dimensional model of the device structure; however, FLOODS can also solve by adding depth to the contact.

Table I. Material (electronic and thermal) properties of Ga_2O_3 vs other semiconductors.

	Si	4H-SiC	GaN (Wurzite)	Ga_2O_3
E_g (eV)	1.1	3.3	3.4	4.6–4.9
μ_n (cm^2/V-s)	1400	1000	1200	100–200
E_{cr} (MV/cm)	0.3	2.5	3.3	8
ε	11.8	9.7	9.0	10.0
Normalized BFOM	1	340	870	1100–2250
κ at 300K (W/m-K)	150	270	210	27 [010] 11 [110]

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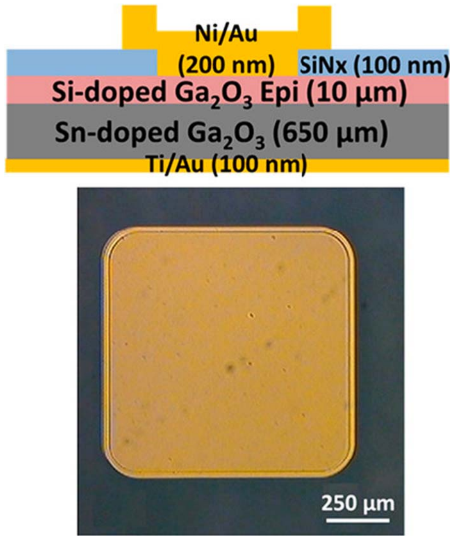

Figure 1. Schematic of vertical geometry Ni/Au Schottky structure (top) and top view, with SiN_x edge termination layer and device area of 0.01cm^2 (bottom).

Device structure.—The basic device structure, given in Figure 1[17] is used as a reference to perform electro-thermal analysis, designed to achieve both high forward currents and good reverse breakdown characteristics.[17–19] In this study, the device structure consists of lightly doped epi-layer grown on bulk Ga_2O_3 with [001] surface orientation, with E-beam evaporated Ni/Au forming the Schottky contact and Ti/Au forming the ohmic contact. The doping concentrations in our simulation for the epi-layer is 1.33×10^{16} cm^{-3} and for the bulk layer is 3.6×10^{18} cm^{-3}, determined through C^{-2}-V characteristics.[17]

Electrical domain.—To accurately model semiconductor device electrical performance, such as I-V relationships, we incorporate trap ionization in the common differential equations that model electrostatics and charge transport in semiconductors. The common device equations include the following:

$$\nabla^2\psi = -\frac{q}{\epsilon}\left[p - n + N_D^+ - N_A^-\right] \quad (Poisson's\ equation) \quad [1]$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.J_n,\ \frac{\partial p}{\partial t} = \frac{1}{q}\nabla.J_p \quad (Continuity\ equations) \quad [2]$$

$$J_n = -q\mu_n n\nabla\phi_{fn},\ J_p = -q\mu_p p\nabla\phi_{fp} \quad (Current\ density\ equations) \quad [3]$$

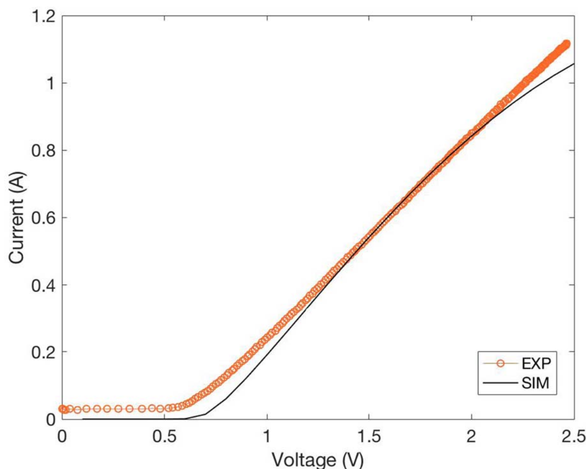

Figure 2. Simulated I-V characteristics compared to experimental I-V using FLOODS TCAD with Schottky barrier height of 1.04 eV.[17]

where ψ is the electrostatic potential, n and p are the respective electron and hole densities, N_D^+ and N_A^- are the ionized donor and acceptor trap densities, respectively, q is charge, ϵ is the permittivity, J_n and J_p are the electron and hole current density, respectively, μ_n and μ_p are electron and hole mobilities, respectively, ϕ_{fn} and ϕ_{fp} are the respective quasi-Fermi levels for electrons and holes. By using the Boltzmann relation, the quasi-Fermi level can be related to the electrostatic potential. The ionized trap states are assumed to be distributed in energy space via a Gaussian.[21] Equation 4 describes the formulation of ionized donor trap density

$$\frac{N_D^+}{N_{tot}} = \int \left(\frac{1}{1+2e^{\frac{E_F-E}{kT}}}\right)\left(\frac{1}{\nabla E\sqrt{2\pi}}e^{-\frac{(E-E_T)^2}{2\nabla E^2}}\right)dE, \quad [4]$$

where $N_D{}^+$ is the ionized donor concentration, N_{tot} is the total donor trap concentration, E_F and E_T are the electron quasi-Fermi levels and trap levels, respectively, and ∇E is the energy spread of the traps. The Full Width Half Max (FWHM) of the distribution is $2\sqrt{2ln2}\nabla E$. The same can be applied to acceptor traps by changing the respective variables accordingly. A conservative energy spread of 0.1eV was used in the simulations. The total trap densities for the lightly doped epi-layer for donor and acceptor traps were 1.5×10^{15} cm^{-3} and 1.75×10^{16} cm^{-3}, respectively. The energy levels were spread throughout the bandgap, with donor traps 0.6, 0.8, and 1.1 eV from the conduction band and acceptor traps at 0.4 and 1.2 eV from the valence band.[22,23]

A Hall mobility model (Eq. 5) has been incorporated using the equations derived in Ma et al.,[24] which takes into account temperature, and the impurities (ionized and unionized) within the material. Figure 2 shows validation of our simulation with a close fit to the experimental forward IV curve for a Schottky barrier diode.[17]

$$\mu_H = \frac{56\left\{\exp\left[\frac{58}{T(K)}\right]-1\right\}}{\left\{1+\frac{N_D(cm^{-3})}{[T(K)-278]*2.8\times10^{16}}\right\}^{0.68}} \quad [5]$$

Thermal domain.—The electro-thermal modeling is performed by incorporating the heat generation term due to Joule heating[25,26] and uses the electron and hole current densities defined in Eq. 3 and to validate the heat transport COMSOL will be used. The heat generation is formulated as:

$$Q = \frac{q\mid J_n\mid^2}{\mu_n n} + \frac{q\mid J_p\mid^2}{\mu_p p}, \quad [6]$$

where Q is the heat generation term.

Heat transport is treated using this heat generation, which is then related to the temperature by a differential equation taking into account the temperature change with respect to space and time.

$$C\frac{\partial T}{\partial t} - \nabla.K\nabla T = Q \quad [7]$$

where C is the specific heat capacity, T is temperature and K is the thermal conductivity. The thermal conductivity for Ga_2O_3 has been studied in detail,[27–31] where the anisotropic thermal conductivity at room temperature has a maximum value of 27.0 ± 2.0 W/mK along the [010] direction to a minimum value of 10.9 ± 1.0 W/mK along the [100] direction.[27] In our simulation, we assume an average isotropic thermal conductivity of 21.0 W/mK. As stated earlier the epi-layer is grown on bulk Ga_2O_3 with [001] surface orientation and a majority of the thermal conductance is likely to be along the [001] direction, and the reported value of thermal conductivity along the [001] direction is 21 ± 2 W/mK.[31] Incorporating anisotropic properties in the FLOODS TCAD simulator has not been achieved yet, and in coherence with previous thermal simulation studies[32,33] isotropic values for the thermal conductivity have been considered. The Kapitza resistance or the Interfacial thermal resistance (ITR) has been ignored in our first-order model although, there have been studies that show a temperature discontinuity at the interface due to the ITR.[34,35]

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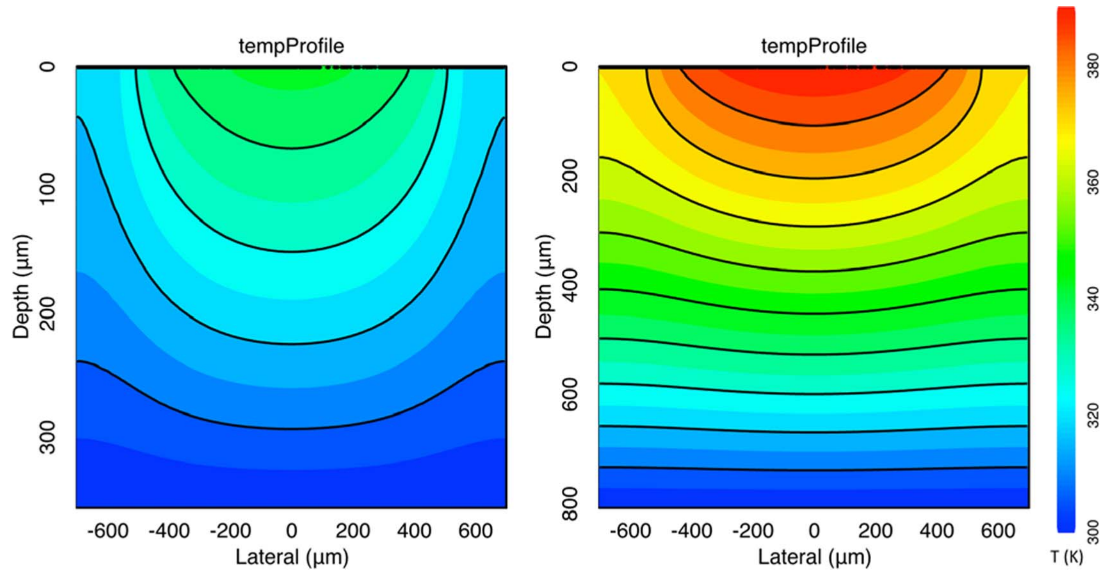

Figure 3. Cross-sectional temperature profile at 2.5V forward bias, with the anode as top contact for bulk thickness 350 μm (left) and 800 μm (right). The epi-layer thickness is constant at 7 μm and the contact area is $0.01cm^2$. Power generated at 2.5V is 4.11W and 2.93W for 350 μm and 800 μm bulk thicknesses respectively and peak temperature values being 342 K for 350 μm bulk and 389 K for 800 μm bulk.

To model the heat dissipation into the atmosphere, convective heat transfer is assumed from the device to its surrounding, or from the heat sinks attached to the device. Assuming that the atmosphere is air with no fluid motion, this results in natural convection from the surface which occurs via the change in density of the fluid from the heating process.[36] To model the heat flow from the solid to the gas, a general equation to define the convective heat transfer given by Newton's law of cooling is used.

$$q' = hA\,(T_s - T_\infty) \tag{8}$$

The equation will be used as a boundary condition for heat flow from the surface to its surrounding, where, q' is the heat flux, h is the heat transfer coefficient, A is the area of the surface, T_s and T_∞ (300K) are the surface and ambient temperatures respectively. The heat transfer coefficient, h, is expressed as a function of a dimensionless number known as the Nusselt number. This Nusselt number, Nu, is further expressed as a function of two other dimensionless numbers, the Grashof and Prandtl numbers (or together known as the Rayleigh, Ra, number).

$$Nu(Gr, \mathrm{Pr}) = hL/k \tag{9}$$

$$Gr = \frac{g\beta\ (T_s - T_\infty)\,L^3}{\upsilon^2} \tag{10}$$

$$Pr = \frac{\mu C}{k} \tag{11}$$

In Eqs. 9–11, L is the characteristic length, k is the thermal conductivity, g is the gravitational force, β is the volume coefficient of expansion (β = 1/T; for an ideal gas), μ and υ are the dynamic and kinematic viscosities. In order to get an expression for the heat transfer coefficient for different surfaces a simpler expression gives a better understanding:

$$\overline{Nu} = \frac{\bar{h}k}{L} = c(Gr\ \mathrm{Pr})^m, \tag{12}$$

where c and m are constants which depend on the type of surface in question. For our case, heat loss via convection from the top and side surfaces have been derived and the expressions have been set as the boundary conditions. Hence, we solve for the temperature of each node created by FLOODS at the required surface and integrate it over the total length (L) of the surface.

Boundary conditions.—Electrical contacts have been implemented at the top (Schottky) and bottom (ohmic) surfaces of the device; and a differential voltage is applied from 0–2.5V for all the cases in our simulations. A Dirichlet boundary condition is applied for the temperature at the back side of the wafer (bottom contact) of T = 300 K, representing that it is in contact with a strong heat sink. The top has Dirichlet boundary conditions for non-convective simulations, while in simulations with convective heat loss, Neumann boundary conditions have been set for the temperature.

Results and Discussion

We simulated different cases that consider the effect of device size and the presence of heat sinks on the electrical performance and the temperature profile in the device cross-section. In the simulations that assessed the effect of dimensionality (i.e. different thicknesses of the bulk and epitaxial layers), the bottom contact of the device was considered to have a strong heat sink (i.e., T = 300 K) and the sides and top of the device had thermally insulating boundary conditions. The simulations assessing the effect of a heat sink incorporated boundary conditions of convective heat transfer for the top contact only, all other contacts (bottom and sides) of the device were the same as the varied-dimensionality simulations.

Dimensionality - bulk thickness.—The bulk layer thickness was varied from 100 μm to 1 mm while keeping the epi-layer thickness and the contact area constant. The temperature profiles of two devices with bulk layer thicknesses of 350 μm and 800 μm at 2.5 V forward bias are compared in Figure 3. A higher maximum temperature value is seen for the device with thicker bulk (800 μm). As the bulk layer is made thicker, there is more volume for the heat to dissipate through before being forced to room temperature at the bottom contact (strong heat sink). The range of maximum temperature (T_{max}) for our study is 313 K for a 100 μm bulk thickness and 417 K for a 1000 μm bulk thickness. This range of temperature causes a mobility variation through equation,[5] as a higher temperature causes the epi-layer electron mobility to degrade, from 218.5 cm^2/Vs at 313K to 128.6 cm^2/Vs at 417K. The increase in temperature with larger bulk is reflected in device performance as decreased current, shown in Figure 4 (top). The thicker the bulk layer, the larger the resistance, thus the current density reduces.

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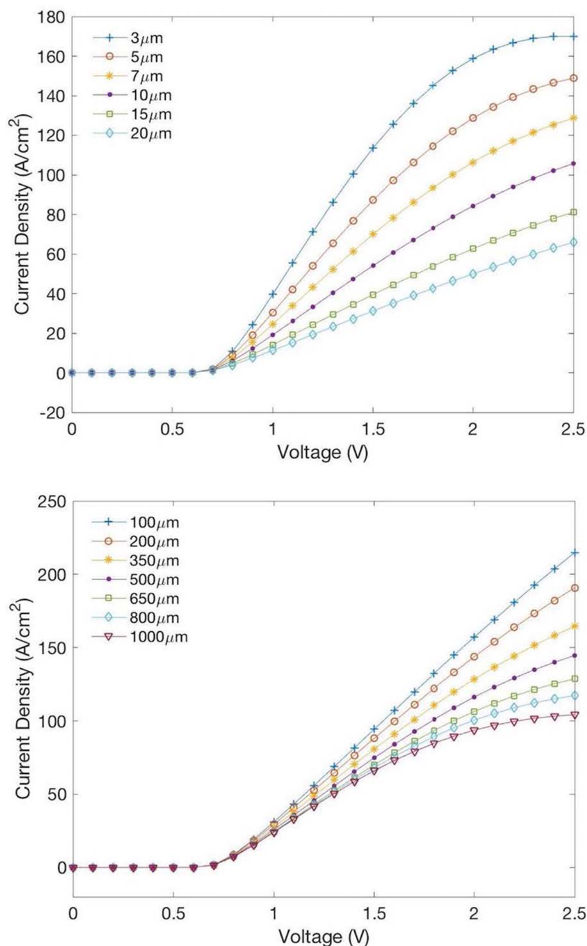

Figure 4. Epi-layer thickness dependence of forward J-V characteristics from 3 μm to 20 μm with a constant bulk thickness of 650 μm (top) and bulk thickness dependence of forward J-V characteristics from 100 μm to 1000 μm with epi-layer thickness constant at 7 μm (bottom).

Dimensionality – epi-layer thickness.—Similarly, the epi-layer thickness was varied from 3 μm to 20 μm, while keeping the bulk layer thickness and contact area constant. As mentioned above, due to low resistance and high mobility, a higher current is achieved for thinner epi-layer structures as shown in Figure 4 (bottom) with the thinner the epi-layer, higher the power generated at 2.5V forward bias.

Figure 5 shows the effect on the temperature profile; the effect of Joule heating is more evident in the thinner epi-layer structures (10 μm, left graph, 3 μm right graph). As the epi-layer is thinned, the resistance decreases and the same current is achieved at lower biases, which in turn results in similar power generation ($P = V^2 / R$) versus the change in temperature curves (Fig. 7 top). However, higher current generation at lower biases results in a higher temperature profile due to Joule heating. The maximum temperature (T_{max}) range for our study is 465 K for a 3 μm epi-layer to 324 K for a 20 μm epi-layer thickness. Due to large temperature range, mobility degradations via equation[5] are noted from 204 cm^2/Vs at 324K to 107.5 cm^2/Vs at 465 K.

In order to realize the true potential of Ga_2O_3 as a material for power applications, thermal management should be prioritized. Due to its low thermal conductivity, k, self-heating effects are evident and efficient heat dissipation should be applied to pacify if not to solve the thermal issues for the device performance. Chatterjee et al.[10] states that dimensionality of the device structure will be important, as the Joule heating from the Schottky contact is seen to be minimized via varying the bulk and epitaxial layer thicknesses.

Figure 6 shows the power and voltage vs the change in temperature while the bulk thickness is varied, whereas Figure 7 shows the power and voltage vs the change in temperature while the epi-layer thickness is varied. The power generated is concentrated in the drift region near the epi-metal interface, and highest temperature values are seen near this interface. Figure 7 (right) shows lines conveying the effect of high volumetric power density in thinner epitaxial layer thicknesses resulting in higher channel temperature values.

Thermal management – heat sinks.—In order to simulate heat loss via heat sinks on the top contact, we used copper heat sinks, as this is the most common material used for heat sinks in the cooling of electronics. This model included the heat loss by free convection on vertical as well as top horizontal surfaces. Fig. 8 shows the temperature profile for 3 test simulations: a) natural convection on a device structure

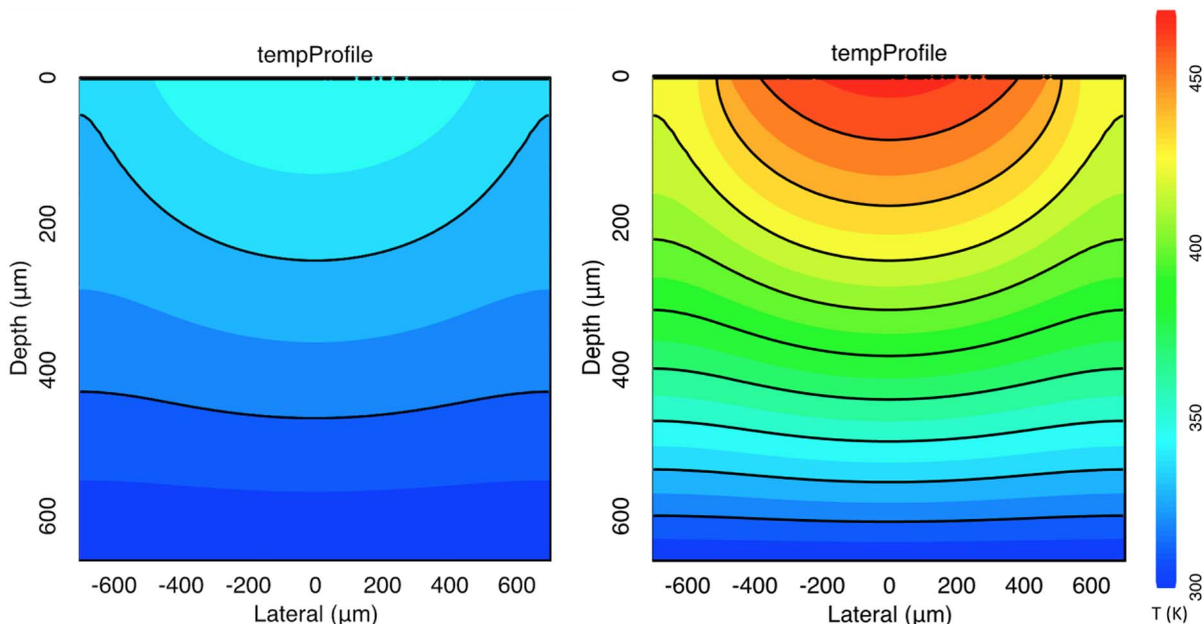

Figure 5. Cross-sectional temperature profile at 2.5 V forward bias, with the anode as top contact for epi-layer thickness 10 μm (left) and 3 μm (right). The bulk thickness is constant at 650 μm and the contact area is 0.01cm^2. Power generated at 2.5V is 4.65W and 2.64W for 3 μm and 10 μm epi-layer thicknesses respectively and peak temperature values being 465 K for 3 μm epi and 349 K for 10 μm epi.

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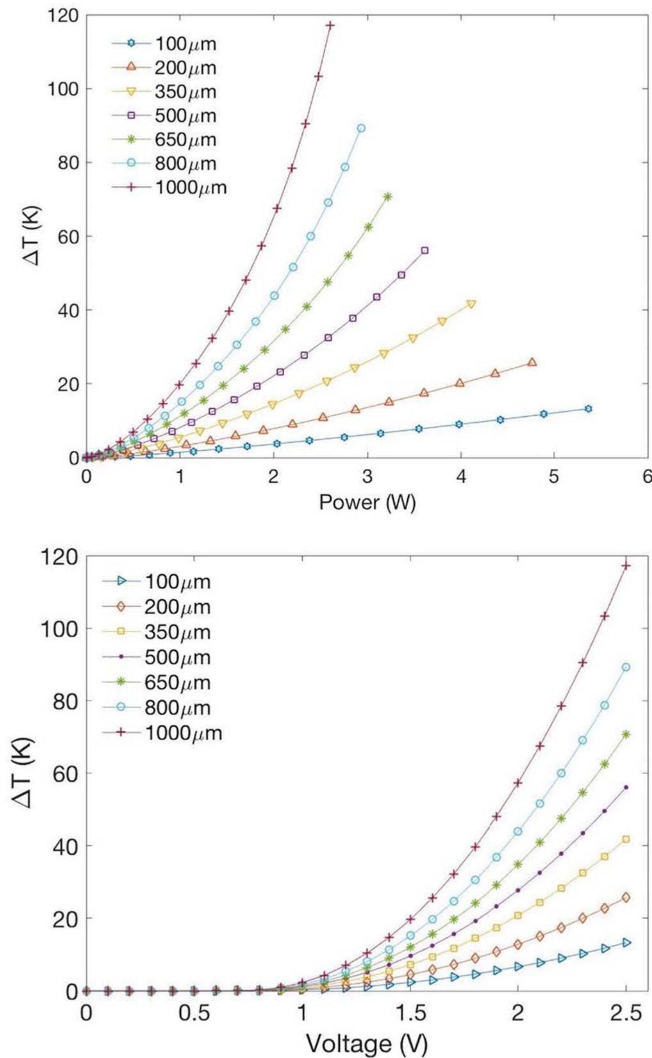

Figure 6. Temperature rise as a function of power (top) and voltage (bottom), while varying the bulk thickness from 100 µm to 1000 µm while the epi-layer thickness is constant at 7 µm.

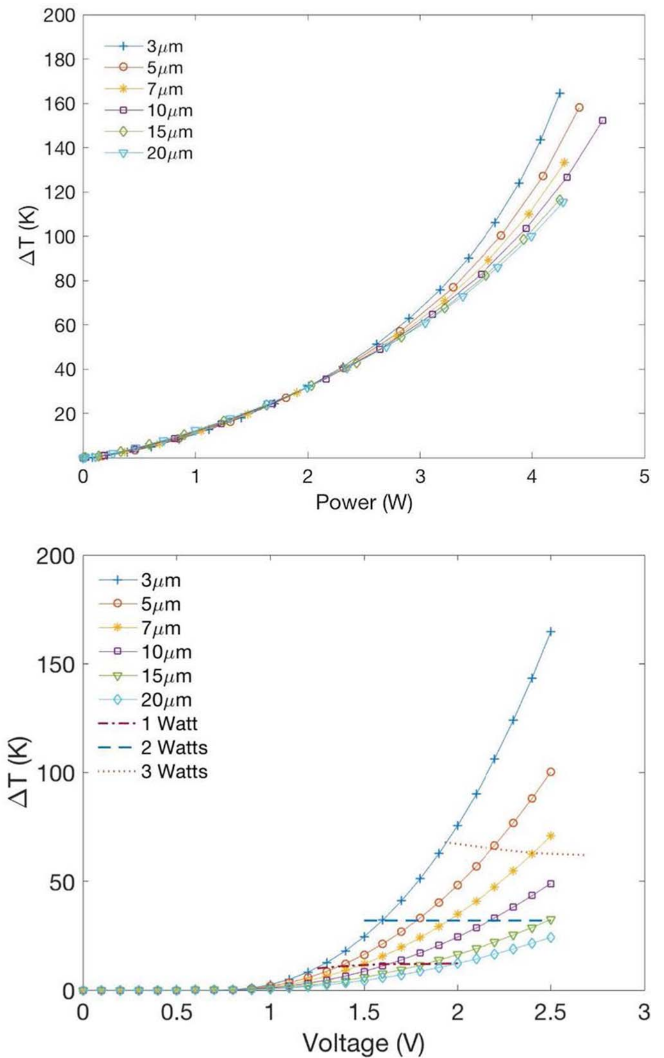

Figure 7. Temperature rise as a function of power (top) and voltage (bottom), while varying the epi-layer thickness from 3 µm to 20 µm while the bulk thickness is constant at 650 µm. The voltage vs ΔT plot includes lines of constant power to shows bias required to reach 1 W, 2 W, and 3 W indicating low bias would be needed for the same current in a less resistive (thinner) epi-layered structure.

with bulk thickness of 650 µm and epi thickness of 7 µm b) the same structure with 1 mm thick solid Cu heat sink on top, and c) the same structure with 1 mm thick Cu and 200 µm thick fins. Compared to the device with no heat sink (Figure 8a), the solid heat sink (Figure 8b) shows a drop of ∼10 K in the T_{max} value, while the heat sink with fins (Figure 8c) shows a drop of ∼25 K in the T_{max} value. This reduction is the T_{max} causes mobility (μ_H) to increase slightly, and that is reflected with higher forward currents. The total heat loss with no heat sinks on top while assuming convective heat loss from the device (Figure 8a.) is minuscule at ∼7 mW.

We also performed simulations that assessed the effects of edge termination (or field plate) and contact area on the forward-bias current and temperature profile. The edge termination (field plate thickness 100nm and 200nm) has little or no effect on the forward bias current as expected; however, field plates are used to boost the breakdown voltage in reverse bias regimes.[17] Simulating while varying the volume under the Schottky contact, by decreasing the contact area from 0.01 cm^2 to 0.0001 cm^2, we notice no change in current density and temperature profile. However, if the bulk volume is wider than the contact area, a decrease in temperature is observed due to more volume for heat to dissipate, hence causing the current density to increase under the contact.

This study addresses an important topic for Ga_2O_3 devices, as the thermal behavior needs to be studied thoroughly and experimental measurements are still in their infancy. Initial thermoreflectance based thermography was done on edge terminated, vertical geometry, Schottky diode devices and, temperature distribution was mapped on the surface of the diode.[37] Furthermore, thermoreflectance thermal imaging (TTI) studies have been done on Ga_2O_3 Schottky barrier diodes,[10] Ga_2O_3 Field-Effect-Transistors[38] and on Ga_2O_3 MOSFETs.[39] These studies are all preliminary thermal measurements and are in good agreement with our simulations.

Conclusions

We have performed a thorough investigation into the effect of device size on β-Ga_2O_3 Schottky barrier diodes, which can aid device optimization. For example, if high power and low self-induced heating is wanted, then the simulation results predict that thin epi and thin bulk layers are needed. The thin epi layer would increase power generation, and the thin bulk would help dissipate that heat generated via the bottom heat sink. Moreover, the low thermal conductivity induces poor heat dissipation and the substrate-side cooling methods fail

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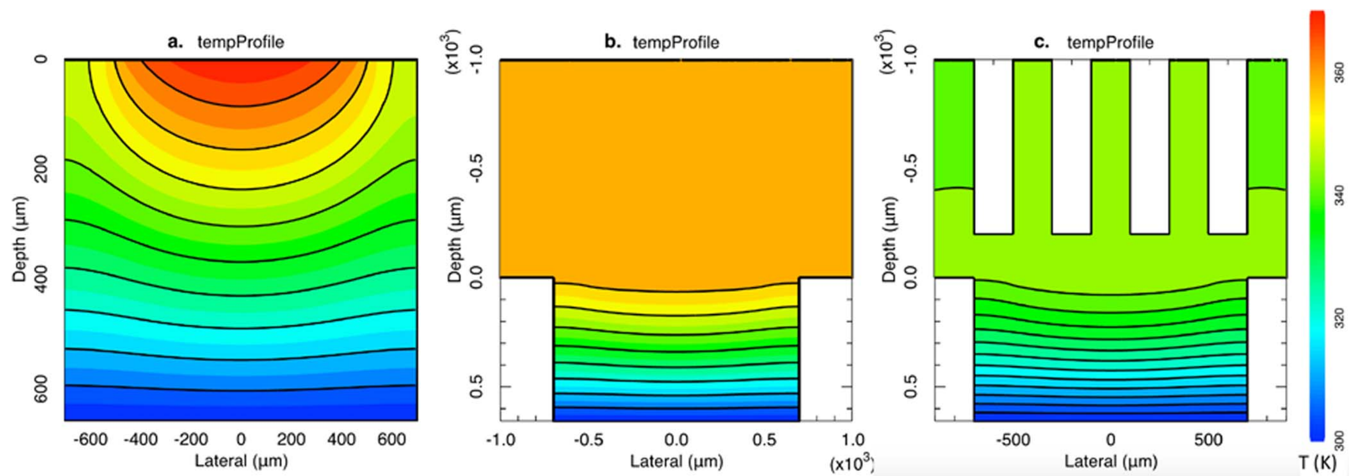

Figure 8. Cross-sectional temperature profile for a diode structure with (a) free/natural convection from device top and side surfaces (peak temperature 369 K), (b) a copper top-side heat sink block (peak temperature 359 K), and (c) a copper top-side finned heat sink (peak temperature 344 K).

to effectively manage the heat generation. We predicted considerable amounts of heat being dissipated near the Schottky contact (anode), and hence the simulation results warrant the requirement of top-side passive cooling, as observed in other studies with top side cooling methods like nanocrystalline diamond capping layers and flip-chip hetero-integration.[10,40,41] The heat sink simulation results show a drop in the maximum temperature as expected. Notably, a copper block heat sink enables a temperature (°C) reduction of 11.34%, while one example of a copper fin heat sink reduced the maximum temperature (°C) by 26.76%. Furthermore, the higher mobility due to lower T_{max} for the copper fin heat sink also resulted in a 5.8% increase in the forward current. These results indicate that different heat sink structures could produce better results and further enhance the heat loss term from the device.

Acknowledgments

The work at UF is partially supported by HDTRA1-17-1-0011 (Jacob Calkins, monitor). The project or effort depicted is sponsored by the Department of the Defense, Defense Threat Reduction Agency. The content of the information does not necessarily reflect the position or the policy of the federal government, and no official endorsement should be inferred.

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