Two New Low-Power and High-Performance Full Adders

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Abstract—**Two new low-power, and high-performance 1-bit Full Adder cells are proposed in this paper. These cells are based on low-power XOR/XNOR circuit and Majority-not gate. Majority-not gate, which produces C_{out} (Output Carry), is implemented with an efficient method, using input capacitors and a static CMOS inverter. This kind of implementation benefits from low power consumption, a high degree of regularity and simplicity. Eight state-of-the-art 1-bit Full Adders and two proposed Full Adders are simulated with HSPICE using 0.18µm CMOS technology at several supply voltages ranging from 2.4v down to 0.8v. Although low power consumption is targeted in implementation of our designs, simulation results demonstrate great improvement in terms of power consumption and also PDP.**

Index Terms—**Full Adder Cell, Majority-not Gate, Low-Power, High-Performance, Power-Delay Product**

I. INTRODUCTION

Arithmetic operations are widely used in most microelectronic systems. Addition is a fundamental arithmetic operation and is the base of many other commonly used arithmetic operations. Therefore, 1-bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. Obviously, improving its performance directly leads to improving the performance of the whole system [1]-[4].

The wide use of this operation in arithmetic functions, have made many researchers eager to propose several kinds of different logic styles for implementing 1-bit Full Adder cell, in recent years [7]-[18].

The most important performance parameters of the VLSI systems are power consumption, speed, and reliability.

Designing low-power VLSI systems has become an important performance goal because of the fast growing technology in mobile computation and communication.

The promotions in battery technology have not occurred as fast as the promotions in electronic devices. Therefore, the designers are confronted with more limitations such as high speed, high throughput and together with consuming as low power as possible. As a result, designing low-power and high-performance Full Adder cells is of great interest [5].

The aim to increase battery life of portable electronic devices is to decrease the energy expended per arithmetic operation, however lower power consumption does not necessarily bring about lower energy dissipation and higher performance. To perform an arithmetic operation, a device can use up very low power by functioning at very low frequency but it may spend a very long time to finish the operation. Therefore, we measure the energy dissipation and evaluate the performance of the system by calculating the Power-Delay Product (PDP), which is the product of average power consumption and worst case delay.

Studies show that Majority-based Full Adders are more reliable than the other common implementations of Full Adder cell [6]. However surveying majority gate-based logic with standard CMOS is not usual, mainly because of the hardware inefficiencies in implementing majority gates. Implementing majority gate based Full Adders with conventional methods bring about a higher number of transistors and consequently lower performance. In this paper, we introduce an efficient method for implementing majority gates, which is more high-performance and efficient, and utilize it for implementing the C_{out} generator part of our proposed Full Adders.

The structure of the rest of this paper is organized as follows; In Section II, we review eight state-of-the-art Full Adder cells. Our proposed Full Adder cells which are presented in section III are compared with these Full Adders. The simulation results of the eight Full Adders and our designs, and also comparisons are presented in

section IV. Finally, Section V contains conclusion.

II. REVIEW OF EIGHT STATE-OF-THE-ART FULL ADDER CELLS

Various static CMOS logic styles have been used to implement low-power and high-performance 1-bit Full Adder cells. In this section eight state-of-the-art Full Adder cells [7]-[13], which our proposed cells are compared with them, are reviewed.

The FA24T of Fig. 1(a) [7] and Bridge of Fig. 1(b) [8] Full Adders are based on a fully symmetric CMOS style, called Bridge style. FA24T has 24 transistors and Bridge has 26 transistors. In FA24T a Bridge circuit generates C_{out} and another Bridge circuit is utilized in series with the prior one to generate Sum, while in Bridge Full Adder, C_{out} and Sum signals are produced in a parallel manner. The body of FA24T has two transistors less than Bridge and has better power consumption. However in FA24T the Sum generator should wait to receive the C_{out} signal from the C_{out} generator, therefore the delay of FA24T is more than Bridge. Although the series structure of FA24T forms a weak driver in the output, however the output inverters provide a good driving power to the cascaded cells. Hence, FA24T has a better drivability than Bridge. The advantages of CMOS Bridge style is higher performance, robustness, and symmetry.

The Complementary Pass-transistor Logic (CPL) Full Adder of Fig. 1(c) [9] has 18 transistors and is based on NMOS pass-transistor network. This causes low input capacitance and high speed operation. However it also leads to one threshold voltage (V_t) loss in the output. CPL consumes less power than standard static CMOS circuits, due to less output voltage swing that is the result of one Vt loss in the output. However it reduces noise margin and causes serious problems in cascading, especially at low voltages. Therefore, CMOS inverters are used to restore the outputs voltage level and ensure the drivability, and feeble PMOS transistors are used to minimize the static current caused by the incomplete turn-off of the PMOS in the output inverters. These overhead devices degrade the performance of the circuit significantly.

The Double Pass-transistor Logic (DPL) Full Adder of Fig. 1(d) [9] is a modified version of CPL and has 24 transistors. Full swing operation is obtained by simply adding PMOS transistors in parallel with the NMOS transistors in DPL circuits. Therefore, the problems of little noise margin and performance degradation at low supply voltages, which occur in CPL circuits because of the output voltage drop, are avoided. However, the addition of PMOS transistors bring about increased input capacitances and performance degradation.

Hybrid [10] and N-CELL1 [11] Full Adders, which are shown in Fig. 1(e) and Fig. 1(f) respectively, are based on low-power XOR/XNOR circuit [14]. Hybrid Full Adder cell, which has 26 transistors, utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively. Although this kind of modification improves the speed of XOR/XNOR circuit, however these additional transistors increase the power consumption of the Full Adder cell. To produce Sum, Hybrid uses another XOR circuit which is implemented with pass transistors. The output inverter restores the output voltage level and improves the driving capability for cascading. The C_{out} generator module of Hybrid Full Adder is a complementary CMOS logic style based MUX. This circuit has the advantages of complementary CMOS logic, which has been demonstrated in [5].

N-CELL1 has 14 transistors and utilizes the low-power XOR/XNOR circuit and a pass transistors network to produce a non full swing Sum signal and uses four transistors to generate a full swing C_{out} signal, which do not provide enough driving power. However N-CELL1 Full Adder cell has 12 transistors less and better performance in comparison with Hybrid Full Adder cell.

Mod2f Full Adder cell of Fig. 1(g) [12], which has 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in [13], this leads to higher speed and better performance in comparison with the circuit proposed in [14]. Then it utilized this circuit together with a pass-transistor network to generate a non full swing Sum signal and with a transmission gate network to generate a full swing C_{out} signal. Due to using pass transistor networks, the output signals of Mod2f do not provide a good driving power.

The last Full Adder which is reviewed in this section is N-10T [13]. Lowering the number of transistors is the advantage of this cell which leads to better performance and less occupied area. However poor driving capability and non full swing nodes are the basic problems of this Full Adder cell. The XNOR node before the inverter and the outputs of the cell have voltage drop.

V_t loss in circuit nodes leads to serious problems especially at low supply voltages, such as very little noise margin, high leakage power, and serious problems in cascading.

III. PROPOSED FULL ADDER CELLS

The functionality of a 1-bit Full Adder cell with A, B, and C_{in} (Input Carry) Inputs, and Sum and C_{out} (Output Carry) outputs, can be described by the following equations:

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}.(A+B) \quad (2)$$

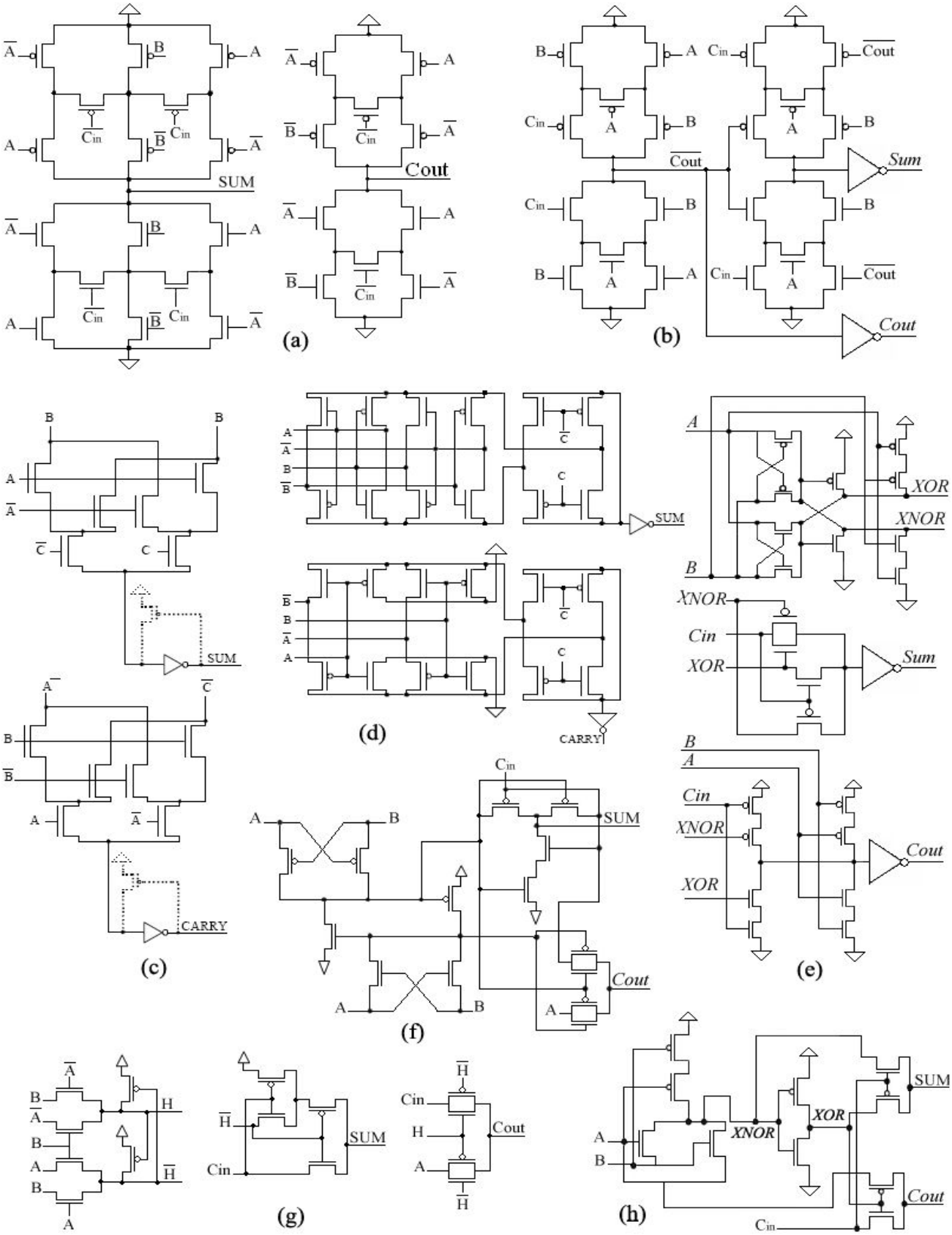

Figure 1. Eight state-of-the-art Full Adder Cells. (a) Bridge. (b) FA24T. (c) CPL. (d) DPL. (e) Hybrid. (f) N-Cell1. (g) Mod2f. (h) N-10T.

As Low power consumption is targeted in implementation of our designs, for implementing Sum circuit, we utilize a low-power 2-input XOR/XNOR circuit [14], which produces XOR (A ⊕ B) and XNOR (A ⊙ B), and a transmission gate based multiplexer [15], which produces $\overline{Sum}$, which is shown in Fig .2. The layout view of Sum generator circuit is illustrated in Fig. 3.

Our new method of C_{out} generating is based on the fact that the functionality of C_{out} function and a 5-input Majority function with A, B, Cin, $\overline{Sum}$ and $\overline{Sum}$ inputs are exactly the same. This fact is based on the following equation and is illustrated in Table I:

$$C_{out} = \overline{Sum}\,.\,(A+B+C_{in}) + A.B.C_{in} \qquad (3)$$
$$= Majority\,(A, B, Cin, \overline{Sum}, \overline{Sum})$$

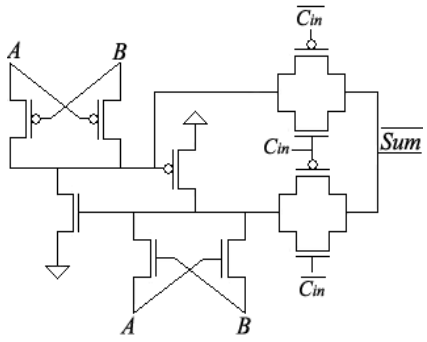

Figure 2. Sum generator circuit

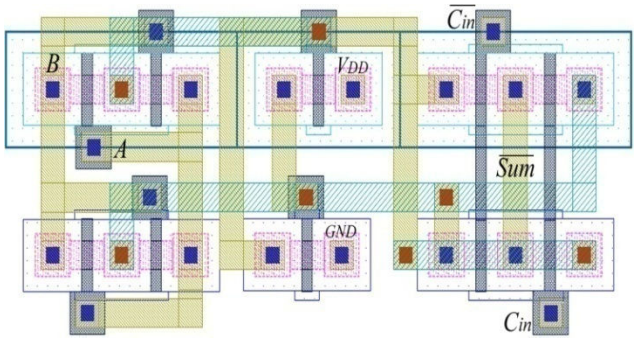

Figure 3. The layout view of Sum generator circuit.

TABLE I.
GENERATING COUT FROM SUM

A	B	C_{in}	$\overline{Sum}$	Maj(A,B,C_{in}, $\overline{Sum}$,$\overline{Sum}$)	C_{out}
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1

Therefore we can produce $\overline{Cout}$ from $\overline{Sum}$ by using a 5-input Majority-not gate as illustrated in Fig. 4.

Conventional implementing methods of Majority gate are not useful here due to hardware inefficiencies. Implementing majority gate with conventional methods bring about a higher number of transistors and consequently lower performance. We introduce an efficient method for implementing a Majority-not gate which uses only small input capacitors and a static CMOS inverter as illustrated in Fig. 5. With this method we can also create majority gates with more inputs by increasing the number of input capacitors.

The capacitor network is used to provide voltage division for implementing majority logic. When the majority of inputs are "0", the output of the capacitor network is considered as "0" by the inverter and consequently the output of inverter is Vdd. When the majority of inputs are "1", the output of the capacitor network is considered "1" by the inverter and consequently the output of inverter is 0v. The inverter also provides a good driving power in the output.

This method enjoys low power consumption, a high degree of regularity and simplicity.

To be distinguished from the other mentioned Full Adders, we called this novel Full Adder "Design1" in this paper.

Although the method of generating C_{out} from Sum by this way is a novel method which provides better VLSI characteristics, we can modify Design1 by producing C_{out} and Sum in a parallel manner.

This method is based on the fact that the functionality of C_{out} function and 3-inputs Majority function, are the same, which can be obtained from (4).

$$C_{out} = A.\,B + C_{in}.\,(A+B) \qquad (4)$$
$$= \text{Majority (A, B, C)}$$

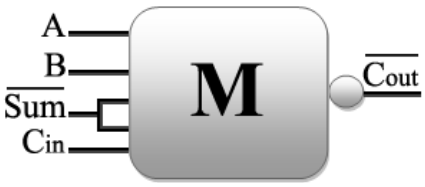

Figure 4. Producing $\overline{Cout}$ from $\overline{Sum}$ by using a 5-input Majority-not gate.

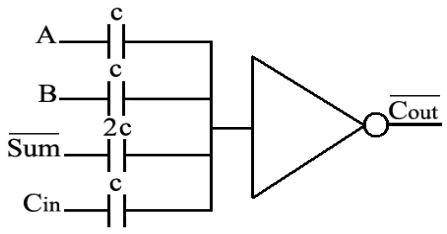

Figure 5. C_{out} generator circuit of Design1.

So we can generate $\overline{Cout}$ separately by using a 3-input Majority-not gate as shown in Fig. 6.

We can utilize the proposed method by using three input capacitors and a CMOS inverter to implement a 3-input Majority-not gate, which is shown in Fig. 7.

By this kind of design, not only the delay of generating C_{out} signal overlaps the delay of generating Sum signal, but also an input capacitor is eliminated, which brings about less input capacitance and subsequently higher performance, higher drivability and less area in comparison with Design1.

To be distinguished from the other mentioned Full Adders, we called this novel Full Adder "Design2" in this paper.

Many realizable alternatives such as Poly-Insulator-Poly capacitors (PIPcap), Metal-Insulator-Metal capacitors (MIMcap), or Metal-Oxide-Semiconductor capacitors (MOScap) can be utilized for implementing the capacitor network. However, MOScap benefits from less chip area, more capacitance, and lower mismatch in comparison with other alternatives and we can utilize it with a comparatively acceptable operation in 0.18µm technology. Usually the PMOScap has higher capacitance than NMOScap for the same area, therefore we chose PMOScap for implementing the capacitor network.

In our designs, it is better to use smaller input capacitors, which leads to better driving, less area and higher performance. The input capacitance of the inverter is measured as about 0.05fF, which is negligible and has no effect on the operation of the circuit.

Larger capacitance brings about more input capacitance and subsequently more delay, more power consumption and larger occupied area. However very small capacitance leads to higher noise sensitivity and realization problems. Another problem with very small capacitance is that the parasitic capacitance becomes considerable and affects the operation and characteristics of the circuit. However, by using higher than 1.4fF capacitance, realized with MOScap, parasitic capacitance of bottom plate in chip realization is not considerable and is negligible.

The layouts of the C_{out} generator circuits of Design1 and Design2 with 2.88fF input capacitors are shown in Fig. 8 and Fig .9 respectively. The layouts show that this structure leads to a dense and simple layout for the complex designs.

The area occupied by a small MOScap is as an ordinary transistor, which is very important for reducing the chip area. The area of Design1 and Design2 cells and the ratio of capacitors area to the total Full Adder area are illustrated in Table II.

Figure 6. Producing $\overline{Cout}$ by using a 3-input Majority-not gate.

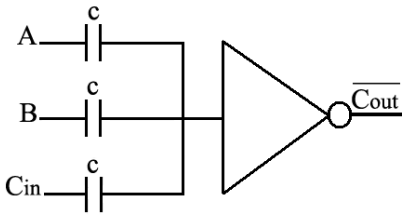

Figure 7. C_{out} generator circuit of Design2.

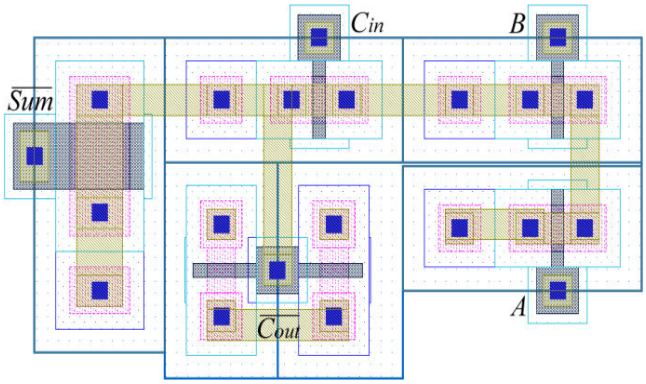

Figure 8. The layout view of the C_{out} generator circuit of Design1.

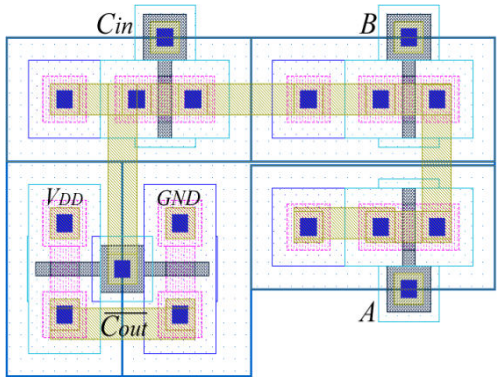

Figure 9. The layout view of the C_{out} generator circuit of Design2.

TABLE II.
AREA OF PROPOSED FULL ADDERS.

Full Adders	Total area (μm^2)	Ratio of capacitors area to total Full Adder area
Design1	82	28%
Design2	73	21%

IV. SIMULATION RESULTS

Eight state-of-the-art 1-bit Full Adder cells including FA24T, Bridge, CPL, DPL, Hybrid, N-CELL1, Mod2f, and N-10T and also our both designs (Design1 and Design2) have been prototyped and simulated. Simulations were done by the aim of minimizing the power consumption by adopting minimum-size transistors. The three inputs have been generated from buffers and have been fed into the adder cell, while the two outputs have been also loaded with buffers (Fig .10). These appropriate inputs and outputs loading provide a more realistic simulation circuit structure.

HSPICE with 0.18µm CMOS technology has been used. The simulations were done for all eight Full Adders and both of our designs in the same condition, at room temperature. The operating frequency is 100MHz and the supply voltage ranges from 2.4v down to 0.8v. A randomly generated input pattern applied to the cells for a long period, for measuring the average power consumption of the cells. The average power consumption of the simulated circuits is calculated by the following equation:

$$P_{avg} = P_{dynamic} + P_{short\text{-}circuit} + P_{static} \quad (5)$$
$$= V_{DD}.f_{clk}.\sum_{i}(V_{iswing}.C_{iload}.\alpha_i) + V_{DD}.\sum_{i} I_{isc} + V_{DD}.I_l$$

$P_{dynamic}$ denotes the switching component of power where, V_{DD} is the power supply voltage, f_{clk} *is* the system clock frequency, and V_{swing} *is* the voltage swing of the output, C_{iload} is the output load capacitance at node i, and α_i is the transmission activity factor at node i.

$P_{short\text{-}circuit}$ represent the short-circuit power, which results from I_{isc} following from power supply to ground at node i, which is negligible due to its small value in our circuits.

P_{static} denotes the leakage power, which is derived from leakage current I_l which is due to reverse-biased junction leakage current and subthreshold leakage current.

Although the P_{static} is low at the range of voltages, which is used for simulating our circuits, it can be a little considerable at lower voltages. However, as our designs have very low $P_{dynamic}$, the average power consumption still remains low.

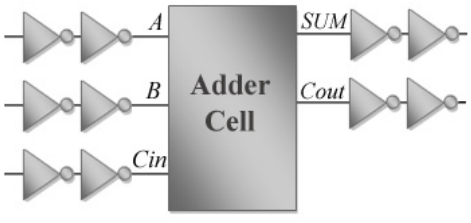

Figure 10. Test-Bed.

The delay of cells has been measured from the moment that the inputs reach 50% of the supply voltage level to the moment that the latest of the Sum and C_{out} signals reach the same voltage level. All transitions from one input to another (56 patterns) have been checked and the delay has been measured for each transition. The maximum has been reported as the delay of each cell. Finally, for performance comparison, the power-delay product (PDP) was calculated by following equation:

$$PDP = \text{Maximum Delay} * \text{Average Power} \quad (6)$$

The simulation results of the proposed designs and the eight state-of-the-art Full Adders, optimized for speed and power, are listed in Table III at four supply voltages.

The delay of Design1 is better than CPL and FA24T at 0.8v and 1.2v. At 0.8v, the delay of Design2 is better than all cells mentioned in table III, at 1.2v it is better than all cells except N-10T, and at 1.8v and 2.4v it is better than FA24T, Bridge and CPL.

The results indicate that Design1 consumes less power in comparison with all eight state-of-the-art Full Adders at all supply voltages, except N-10T at 0.8v and 1.2v and is more high-performance compared with eight state-of-the-art Full Adders at all supply voltages except Bridge at 1.2, and N-CELL1 and N-10T. The power consumption and PDP of Design 2 is less than all other cells mentioned in Table III at all supply voltages.

The Delay, Power consumption, and Power-delay product charted versus supply voltages of the eight Full Adders and our Designs, are shown in Fig. 11, Fig. 12 and Fig. 13, respectively. As illustrated, the power consumption of Design 1 and Design 2 increases slower, with the supply voltage, than the other eight Full Adders.

V. CONCLUSION

Two novel low-power and high performance 1-bit Full Adder cells have been proposed. Both cells use a transmission gate based multiplexer to generate Sum. The first cell produces C_{out} from Sum by using a 5-input Majority-not gate and the second cell which is a modified version of the first one produces C_{out} separately by using a 3-input Majority-not gate to improve the VLSI characteristics of the circuit. Majority gates have been implemented with an efficient method. This method uses only input capacitors and a CMOS inverter. Simulations were done at several supply voltages, ranging from 2.4v down to 0.8v. Although low power consumption has been targeted at the circuit design level for both cells, simulation results show great demonstrated improvement of proposed cells in terms of power consumption and also PDP, in comparison with the eight modern Full Adder cells.

TABLE III.
SIMULATION RESULTS.

Vdd(V)	0.8	1.2	1.8	2.4
Power(*10^{-7}W)				
Design1	2.551	5.691	10.02	17.05
Design2	1.162	3.265	7.743	12.34
FA24T	2.660	5.847	16.69	30.25
Bridge	3.329	7.119	16.67	30.48
N-Cell1	2.941	6.484	16.22	31.22
DPL	4.450	9.704	23.57	42.54
Hybrid	3.993	8.874	22.36	39.26
N-10T	2.185	4.782	13.90	28.68
Mod2f	4.361	9.431	22.38	37.31
CPL	5.3103	9.616	25.45	39.61
Delay(*10^{-10}S)				
Design1	2.257	2.012	1.721	1.317
Design2	1.265	1.142	0.917	0.754
FA24T	2.780	2.093	1.379	1.114
Bridge	2.043	1.510	1.042	0.867
N-Cell1	1.810	1.244	0.632	0.513
DPL	1.604	1.168	0.753	0.601
Hybrid	1.825	1.370	0.806	0.632
N-10T	1.571	1.121	0.735	0.572
Mod2f	1.804	1.305	0.877	0.729
CPL	2.754	2.227	1.411	1.169
PDP (*10^{-17}J)				
Design1	5.757	11.45	17.24	22.45
Design2	1.469	3.728	7.100	9.304
FA24T	7.394	12.23	23.01	33.69
Bridge	6.801	10.74	17.37	26.42
N-Cell1	5.326	8.069	10.25	16.01
DPL	7.139	11.33	17.75	25.56
Hybrid	7.287	12.16	18.02	24.81
N-10T	3.432	5.361	10.22	16.40
Mod2f	7.868	12.31	19.62	27.19
CPL	14.62	21.41	35.91	46.31

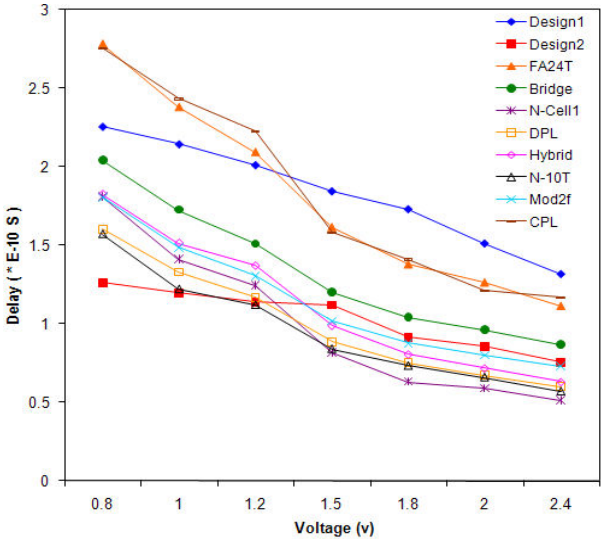

Figure 11. Delay of the cells, versus supply voltage.

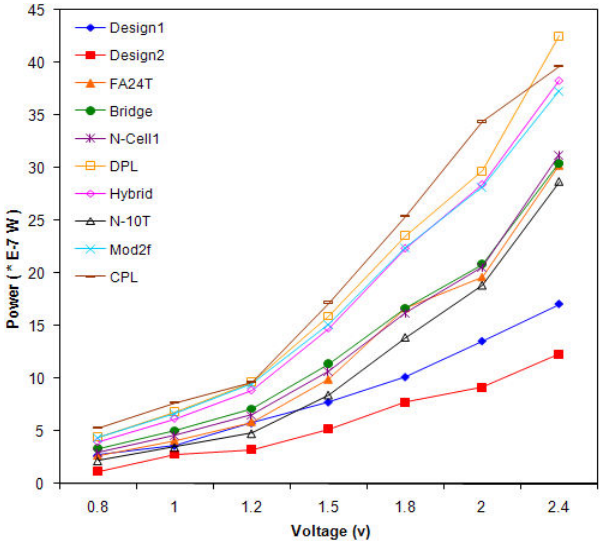

Figure 12. Power Consumption of the cells, versus supply voltage.

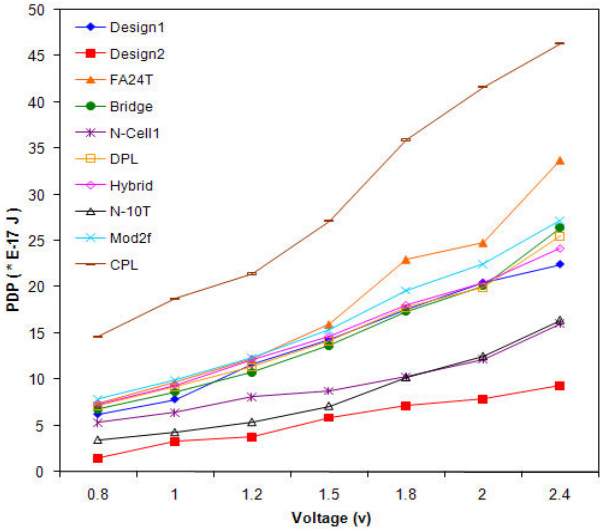

Figure 13. PDP of the cells, versus supply voltage.

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