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A NEW INTERLEAVING TECHNIQUE FOR VOLTAGE RIPPLE CANCELLATION OF SERIES-CONNECT PHOTOVOLTAIC SYSTEMS*

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The research into series connection of dc–dc converters has been concentrating more recently on creating a high voltage low current string. However, the interleaving technique of series-connect photovoltaic (PV) module integrated converters (MICs) has not been sufficiently addressed so far. This paper proposes a low cost high performance interleaving technique based on series PV MICs to reduce the output voltage-ripples. With the reduced voltage-ripples, the size and cost of capacitors at grid connected inverters can be reduced. The proposed technique is capable of solving the problem for PV panels with mismatched operating conditions. Each PV panel is able to track its own maximum power point (MPP) which simultaneously delivers the maximum power for the system. The proposed technique is mathematically investigated based on boost (step-up) converters and validated by Simulink/Matlab simulation and experiment results. The MPP tracking (MPPT) algorithm is tested for a PV/battery charging system with satisfactory performances in both steady-state and transient responses with reduced voltage-ripples.

Keywords: Series dc–dc converters; interleaving technique; MPPT; PV; MIC; voltage ripple reduction.

1. Introduction

During the last few decades, global electric energy consumption has continuously increased. Renewable sources, such as wind and solar, are becoming more and more important due to the serious environmental impacts of conventional fossil fuel sources. Photovoltaic (PV) sources are becoming attractive due to their low maintenance cost, no noise, no installation area limitation.[1] To meet high load-current

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requirement, parallel connection of PV module integrated converter (MIC) has been a subject of vigorous research.[2–5] Due to the multiple input configurations, current-ripples from each MIC will be added together at the load side to form relatively large ripples. Even though the ripples can be reduced by increasing switching frequency, the extra switching losses will result in lower efficiency of the systems. Hence, the interleaving technique is necessary for ripple-cancellation applications. Since the earliest interleaving technique[6] was proposed in 1971, a number of improvements have been addressed[7–11] for only one input source with several parallel converters. The concept of phase shift is adopted and the shift angle is conventionally determined by $2\pi/N$, where N is the number of MICs. However, the interleaving technique applied to multiple input sources has been getting more attractive in recent years based on parallel connected MICs to reduce the current-ripple at the array output side, especially for renewable sources.

Unlike traditional power sources, renewable sources always work under mismatched conditions. The output characteristics of a PV system are crucially influenced by the solar radiation, temperature, load condition or partial shading condition,[12–15] in these cases each PV MIC also tracks its own maximum power points (MPPs). Therefore, the interleaving technique, which considers the different voltages and duty cycles are necessary for the multiple input PV MICs. Several recent topologies have been proposed.[16–19] Power sources, allocated in parallel by using the coupled transformer to implement the multiple input purposes are achieved[16] with the concept of time sharing. Even though the interleaving method of the double input sources having different voltages and different duty cycles is implemented,[16] due to the limitation of the time sharing concept, it can only allow one source to deliver power to a load within one time interval. It is more important for energy sources to deliver power from the source-side to the load-side simultaneously. A phase-shift Pulse-Width Modulation (PWM) control scheme[18,19] is proposed to deliver power from multiple input sources to load simultaneously by using a multi-winding transformer. However it increases the size and cost because of the need for more switches and controllers. Dynamic response is another challenging issue of interleaving techniques. As discussed in previous work,[20] the control duty cycle is updated every four switching periods,[21] therefore the dynamic response becomes sluggish. A fast response requires the correction within one or two switching periods.[20] A flip-flop-based interleaving technique method is proposed[22] to achieve good performances on dynamic responses. However, the control signals are generated based on the detection of rising/falling edges of switching gate signals. The method becomes sluggish at high switching frequency operations because of the fast sampling requirement and a relatively expensive microcontroller is needed.

Compared with paralleled MICs, series connection of MICs is becoming more important recently.[20–24] These can be grouped into three categories: (1) Input-series schemes directly interface with dc-bus. A previous example[20] shows that the grid-connected inverters' input voltage usually ranges from 180 to 500 V. Therefore, a

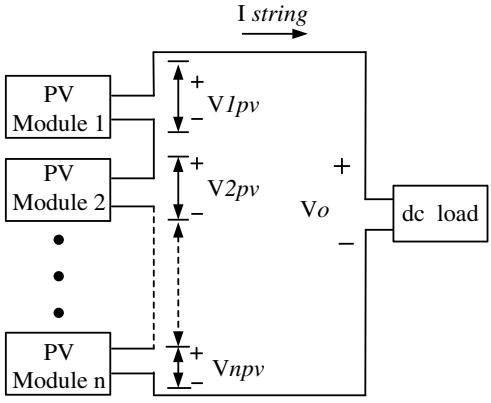

Fig. 1. Series connected PV panel string.

number of PV modules are usually connected in series to supply the inverter with an input voltage within its operating range, which is shown in Fig. 1. Series connection of MICs is suitable to form a high enough voltage for interfacing with the dc bus. (2) Input-series output-parallel (ISOP) schemes.[21] The series connected MICs are integrated with PV panels to form a string. In addition to one string, which consists of a number of PV sources, several strings are capable of being further paralleled at the load side to form the ISOP configuration to achieve higher power delivery. (3) Another connection[22] is input-series and output-series (ISOS) which achieves equal sharing of both input voltage and output voltage.

Although interleaving techniques proposed to date reduce the load-side current-ripples for parallel MICs, the interleaving technique between series connected MICs for PV systems have not been sufficiently addressed. As can be seen in Fig. 2, the string output voltage V_o is the sum of the individual voltages ($V_1, V_2, \ldots$, and V_n) of

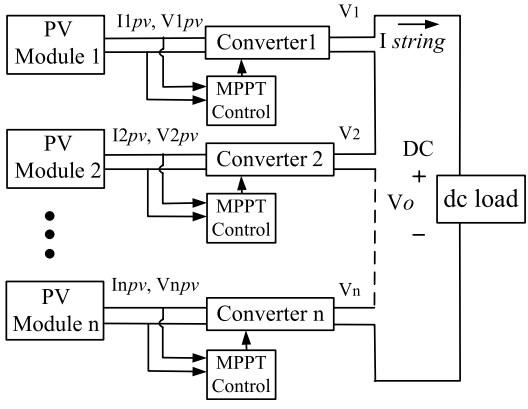

Fig. 2. Series-connect MICs of PV–converter–dc load scheme.

MICs, where the voltage-ripple of V_o is able to be reduced by properly interleaving between each MIC. Due to the voltage-ripple of V_o being reduced at the dc input of the grid-connected dc–ac inverter, the capacitor size and cost can also be reduced.

The proposed method is based on the scheme shown in Fig. 2, which is also able to be applied to ISOP and ISOS schemes with low voltage-ripples on the dc voltage side. In this paper, the research is mainly based on the PV–converter–dc load configurations[23] with reduced voltage ripples at load side. Applications for PV system supplying dc loads are also popular, which is presented in the most recent paper.[24] The proposed interleaving method can achieve reduced voltage ripples so that dc-load cannot receive relatively large voltage fluctuations. It is generally used for stand-alone system to provide reduced ripple voltage for dc loads. Its applications can be PV supplied dc motors,[25] dc/PMDC water pump systems,[26] PV-fed LED lighting systems,[27] PV/battery systems for portable electronic devices,[28] and so on.

The PV sources, with each coupled to its dc–dc converter, are cascaded on the same dc bus and interfaced to the grid by means of a dc–ac inverter. In this paper, the proposed interleaving method is based on the well-known distributed MPPT (DMPPT) configuration, which has been well documented.[29–33] Local MPPT is applied to each PV panel to deliver the maximum power from the input side to the load simultaneously. As discussed in previous literature,[31] traditional centralized or string MPP tracking (MPPT) system, all PV panels connected in series are forced to drive the same current, which results in mismatching problems with MPPT. The other well known alternative is ac module for each PV panel.[34] However, it is quite difficult to reach the grid voltage from the single PV source.[31] Therefore, DMPPT configuration is adopted in this paper for the proposed interleaving method, as shown in Fig. 2.

In DMPPT configuration, MICs remove losses due to the mismatch between panels and support panel level MPPT. As discussed in previous literature,[35] considering the mismatch loss together with the MIC conversion loss contributing to the whole PV system loss, it is very important to notice that converters' internal losses will affect the overall PV system efficiency.[36] Also the string/centralized configurations may have lower system efficiency than MICs due to higher mismatch loss although they usually have higher power conversion efficiency than MICs. For detailed investigations and comparisons of MICs for PV system efficiency can be found in literatures.[37,38] Regarding the limitation of DMPPT, DMPPT systems have the problem regarding the output voltage distribution in the dc/dc converters. However, our work only proposes the interleaving technique, which is based on DMPPT with reduced voltage ripples for dc loads. The limitation and improvement for DMPPT configuration are not the scopes of this paper.

The theoretical analysis in this paper is based on the shift of PWM signals without change of duty cycle (value) to converters. Converter efficiency also changes with different duty cycles and duty cycle values depend on the solar irradiations so that the MPP occurs at different power point. Then, any converter losses will remain the same and PV system overall efficiency will also remain the same in this paper.

Compared with the conventional interleaving technique,[20] in which case the control duty cycle is updated in four switching periods, the proposed technique achieves a fast dynamic response so that the control duty cycle is updated within only one switching period on transit and step-response tests. The voltage sharing in a PV/Battery system is also analyzed in this paper.

The organization of this paper is listed as follows: Section 2 describes the operation principle of the proposed switching technique for voltage-ripple cancellation. Mathematical analysis is given to theoretically prove the proposed technique. Voltage sharing between PV MICs is analyzed. Simulation and experimental verifications are shown in Sec. 3. Boost converters are considered in this paper as they are the most efficient topologies for a given cost.[39] The most favorable advantages are summarized in Sec. 4. A detailed discussion is given in Sec. 5, which considers the PV MICs efficiency, MPPT efficiency, multiple PV MICs and the possible ISOP/ISOS implementations.

2. Principle of Operation

2.1. *Switching technique description*

2.1.1. *Series boost MICs*

The analysis of the proposed interleaving technique starts from two series connected MICs, and then moves to multiple series connected MICs in Secs. 2.2 and 2.3. As can be seen in Fig. 3, two PV sources, each coupled to its boost dc–dc converter, are cascaded on the same dc bus. The output voltage V_o is the sum of voltages V_1 and V_2 from two boost converter output voltages. Current values I_1, I_2 and I_3 remain the same values due to the nature of the series connection configuration.

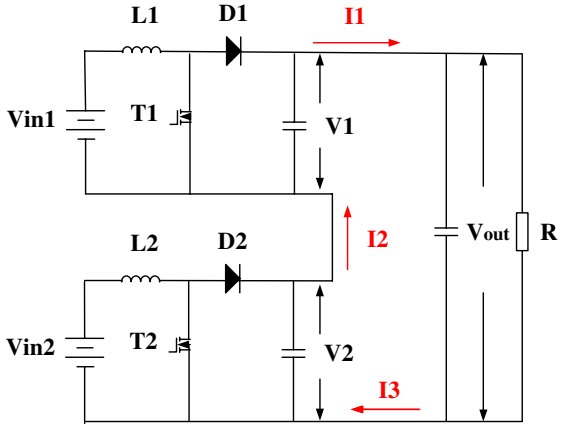

Fig. 3. Series connected two boost-type MICs scheme (color online).

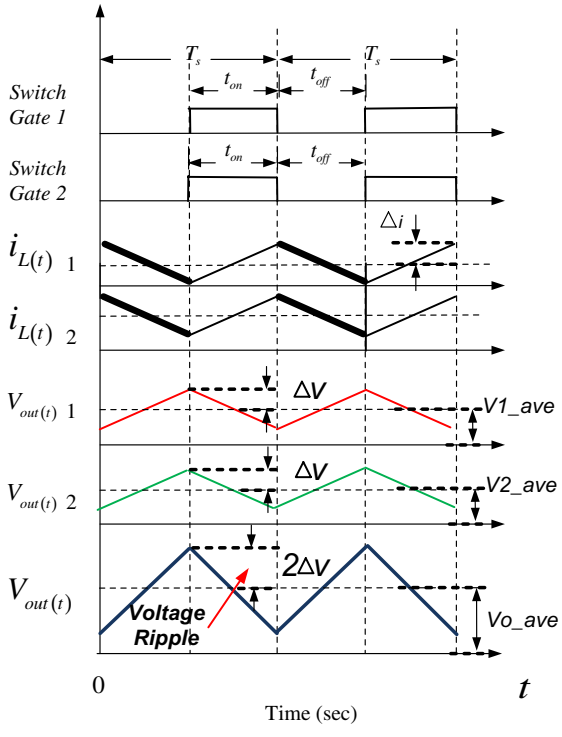

Fig. 4. Key waveforms of typically uncontrolled series connected MICs, ($d_1 = d_2 = 0.5$) (color online).

Hence, voltage average values and ripples of V_1 and V_2 form the waveform of V_{out} at the load side to the dc bus. Typical voltage waveforms, V_1, V_2 and V_{out} without interleaving are given in Fig. 4. For simplicity, as can be seen in Fig. 4, the values of the two duty cycles are both assumed to be the same ($d_1 = d_2 = 0.5$). V_{out1} and V_{out2} are the two boost-converters' output voltages. V_{out} is the voltage, obtained from the sum of V_{out1} and V_{out2}, which forms the dc-bus voltage. The voltage-ripples V_{out1} and V_{out2} are in phase with each other, which are added up at the dc-bus side to form a doubled voltage-ripple of V_{out}. The assumption shown in Fig. 4 illustrates that uncontrolled series MICs can form a large voltage-ripple at the dc-bus side if there are a number of series MICs providing a desired voltage. Basically, voltage from each boost-converter is able to be shifted by properly shifting the inductor current. The phase-shift of the inductor current can be controlled by switching gate signals. Hence, phase-shift control of the inductor current is employed in order to interleave the output voltages between each series MIC. With the same assumption as shown in Fig. 4, $d_1 = d_2 = 0.5$ for two boost-converters, a suitably shifted inductor current can result in the interleaving of the two voltages V_{out1} and V_{out2}.

As described in Fig. 5, inductor currents of two boost-converters are shifted within one switching period. When the switching gate 1 is "on", the inductor current

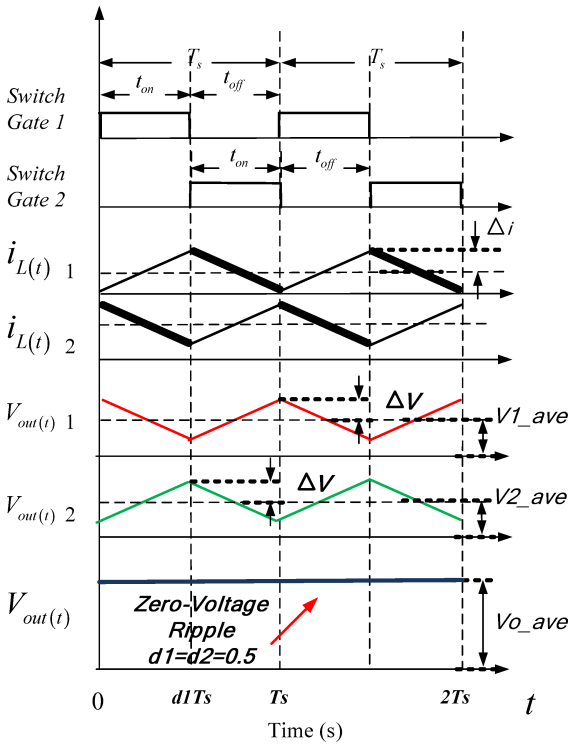

Fig. 5. Key waveforms of the proposed interleaving operation between series boost MICs ($d_1 = d_2 = 0.5$) (color online).

i_{L1} keeps increasing until the switching gate 1 is "off". Therefore, the peak of inductor current i_{L1} occurs at the same time instant when discharging starts. In other words, the peak of i_{L1} always occurs when the switching gate 1 starts to turn "off". At the same instant when gate 1 is "off", gate 2 starts turning "on" with the peak of i_{L2} occurring at the same instant as the peak of i_{L1}. Consequently, by controlling the inductor currents i_{L1} and i_{L2}, boost-converter output voltages V_{out1} and V_{out2} are satisfactorily shifted as shown in Fig. 5. Hence, the zero voltage-ripple on the dc-bus side can be achieved due to the interleaving between two series boost-converters, which is the most desired voltage-ripple cancellation of two MICs operating with the same source voltages and same duty cycles ($d_1 = d_2 = 0.5$).

2.1.2. *Different duty cycle analysis*

Unlike traditional dc-sources, for example batteries, PV sources are commonly not identical in size and operating conditions. Furthermore, because MPPT algorithms are applied individually to each PV panel, they may work on different duty cycles and voltage levels. Three main geometric circumstances[40] that result in the

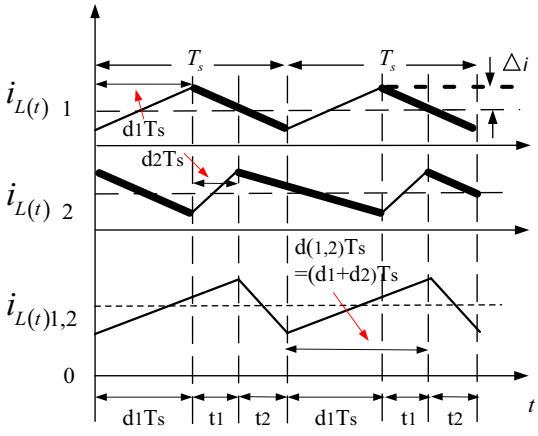

Fig. 6. Two inductor currents from each MIC i_{L1}, i_{L2}, and the second generation current obtained virtually from the sum of i_{L1} and i_{L2} (color online).

non-uniformities on the PV systems are usually taken into account: (1) different cell orientations in a series PV MIC string. For example, the installation of PV on a gabled residential roof with different facing directions can produce a significant variation in beam radiation; (2) shadings to a portion of a string cause radiation non-uniformities; (3) differences of the reflected radiation from nearby objects. The key waveforms of a series MIC string consists of two converters are described in Fig. 6. As discussed in the previous section, boost and buck converters have the same relationship between switching gate signals and inductor currents. Therefore, the proposed generalized implementation of phase shifting is suitable for both types of converters. In this paper, only boost converter is investigated mathematically with simulation and experiment verifications. When inductor currents are properly shifted, voltage-ripples are cancelled accordingly. In addition, due to the inductor currents being used only for control purposes, it is not necessary to really sense current values. Only the duty cycles are adopted for calculation of the second generation duty cycles.

As can be seen in Fig. 6, the peaks of i_{L1} and i_{L2} cancel each other out at the same instant in time, which creates a new generation of inductor current with a new duty cycle. The current $i_{L1,2}$ is realized as the "virtual" waveform of the second generation current obtained virtually from the sum of the inductor currents i_{L1} and i_{L2}, which are only adopted for the control purposes, because there is no circuit loop passing through the combination of i_{L1} and i_{L2} in series connection. Therefore, after obtaining the second generation current, the new duty cycle d_{1-2} is carried out for phase shift determination with other converters. The series MICs scheme is proposed for two converters, which gives the new value of the second generation duty cycle as:

$$d_{1-2} = d_1 + d_2\,, \tag{1}$$

where the duty cycle d_{1-2} must be limited within the range 0–1. Hence, once the value of the duty cycle exceeds 1, the new duty cycle is given by

$$d_{1-2} = d_1 + d_2 - 1\,. \tag{2}$$

By properly shifting the second generation current, the peaks of the voltage-ripples from all MICs are shifted and thus reduced. The second generation is analyzed in this section, and the extensions of the proposed technique of voltage-ripple cancellation from 2 to n MICs are explained in Sec. 2.3. All the MICs are grouped in pairs with one "Master" and one "Slave". The next generation "virtual" current is further considered as either "Master" or "Slave" for further cancellations.

2.1.3. *Multiple input "n" MICs analysis*

The proposed voltage-ripple cancellation technique requires "Master" and "Slave" converters grouped in pairs. Master–Slave scheme has been widely adopted. The research works based on Master–Slave scheme are well documented in previous literatures.[41–43] The scheme is also getting popular in industrial products.[44,45] As shown in Fig. 7, converter 1 is considered as the "Master" converter, based on which the "Slave" converter 2 shifts the inductor current i_{L2} according to the cancellation procedure. Then, the second generation is obtained with the second generation duty cycle. Hence, the converter 3 is considered as a second generation "Slave" converter to cancel the peak of "Master" second generation 1, as shown in Fig. 7. Note that all the cancellations are based on the peaks of inductor current-ripples, accordingly the voltage-ripples can be shifted to the same phase angle and cancelled satisfactorily.

Since the proposed interleaving method is based on Master–Slave scheme, it is apparent that for this Master–Slave-based interleaving method, "Slave" converter switching gate signal will shift according to the "Master" converter. When the "Master" converter fails, slave converter will fail to implement. However, as presented in Fig. 7, if "Master" converter fails, the other converter (Slave) will lose the

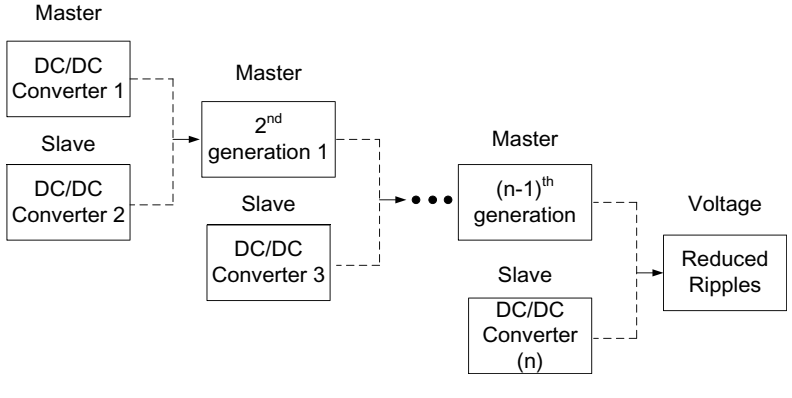

Fig. 7. The proposed interleaving technique to reduce dc-bus voltage-ripples of "n" series MICs scheme.

shifting, but it remains the same duty cycle for further generation voltage ripple cancellation. Since boost converters can provide the circuit as a pass-through current loop, duty cycles can be set to be 1 and 0 respectively when a fault of PV module is detected. Fault to "Master" converter will not affect the interleaving implementations for other Master–slave pairs thanks to the proposed method being strictly based on pair's ripple-cancellation.

2.1.4. *Implementation of the proposed technique*

Hardware-implementation of the proposed technique employs the Exclusive-OR logic circuits. To implement the proposed switching technique in simulation and experimentation, the Exclusive-OR logic circuits are employed as shown in Fig. 8.

In order to shift the angle of Gate 2 for d_1T_s from Gate 1, the generated Gate 2 is based on the operation of the principle shown in Figs. 9 and 10. As can be seen in Fig. 9, Y_1 is obtained from the Exclusive-OR between Gate 1 and B1 ($d_1T + d_2T$). If $d_1 + d_2 \leq 1$, the duty cycle of PWM_3 is set as $d_1T + d_2T - 1 = 0$. Hence, the Gate 2 with phase shift d_1T is obtained as Y_2, as shown in Fig. 9.

Similarly if the value $d_1 + d_2 > 1$, the signal B1 is set as $d_1T + d_2T = 1$, and the signal B2 is given by the PWM_3 with duty cycle $d = d_1T + d_2T - 1$. Hence, the Gate 2 with phase shift d_1T can be successfully obtained as Y_2, as shown in Fig. 10.

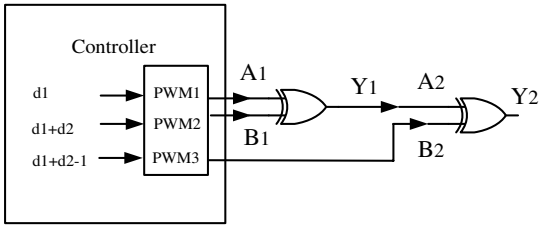

Fig. 8. Implementation of the proposed switching technique.

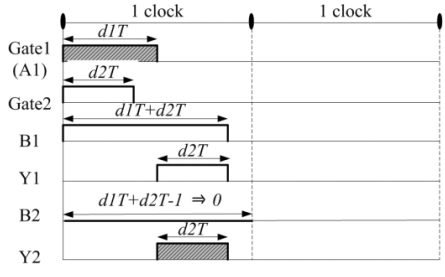

Fig. 9. Operation of the switching signals ($d_1 + d_2 \leq 1$).

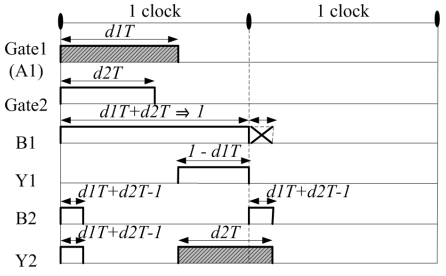

Fig. 10. Operation of the switching signals ($d_1 + d_2 > 1$).

2.1.5. *Voltage sharing investigation*

As all the MICs are in series, output voltage from each converter is individually adjusted locally. Even though the dc-bus voltage is well known as the sum of all the output voltages from MICs, voltage sharing issues are necessarily addressed in this series MICs scheme. The analysis is based on the series boost MICs. As shown in Fig. 3, the output voltages V_1 and V_2 of the two boost converters are

$$V_1 = \frac{V_{\text{in1}}}{1 - d_1}\,, \tag{3}$$

$$V_2 = \frac{V_{\text{in2}}}{1 - d_2}\,, \tag{4}$$

where the V_{in1} and V_{in2} are the two input voltages. d_1 and d_2 are the duty cycles of the boost converters. Two currents I_1 and I_2 are given by

$$I_{\text{in1}} \cdot (1 - d_1) = I_1\,, \tag{5}$$

$$I_{\text{in2}} \cdot (1 - d_2) = I_2\,. \tag{6}$$

Since it is a series connection, $I_1 = I_2$. Hence, the ratio of the input powers P_1 and P_2 are

$$\frac{P_1}{P_2} = \frac{V_{\text{in1}} \cdot I_{\text{in1}}}{V_{\text{in2}} \cdot I_{\text{in2}}} = \left[\frac{V_1 \cdot (1 - d_1)}{V_2 \cdot (1 - d_2)}\right] \cdot \frac{1 - d_2}{1 - d_1} = \frac{V_1}{V_2}\,, \tag{7}$$

and the ratio of the converter output voltages are directly proportional to the ratio of input powers. Therefore, the PV panels working at MPPs provide the maximum power to the dc-bus side, where the voltages from the converters have the same ratios of MPPs of the PV panels. The theoretical analysis of the proposed interleaving technique for series MICs schemes will be further verified in the simulation and experiment results in Sec. 3.

3. Simulation and Experiment Verifications

The parameters of boost converters are listed in Table 1. Three PV sources are tested with the perturbation and observation (P&O) MPPT algorithm implemented. The

Table 1. The circuit parameters.

dc–dc converter parameters	Value	Unit
Inductor (L)	220	μH
Capacitor (C)	22	μF
Switching frequency	30	kHz
dc-bus voltage	48	V

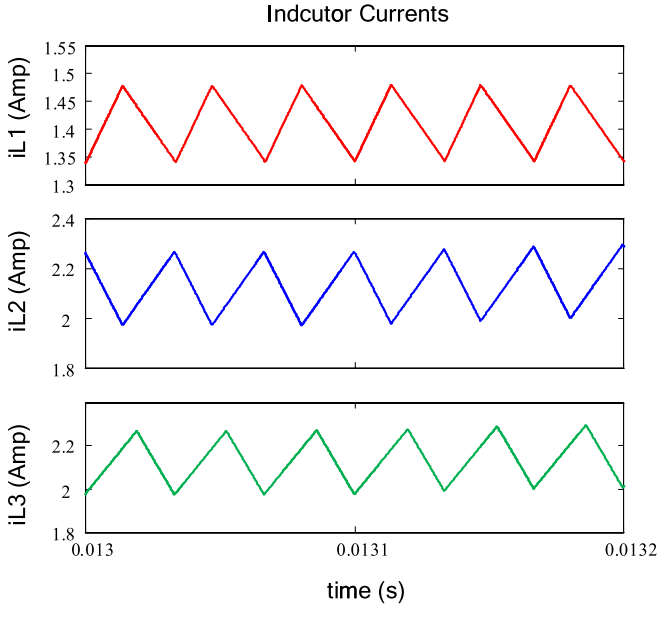

Fig. 11. Inductor currents of series converters: i_{L1}, i_{L2} and i_{L3} (color online).

interleaved inductor currents i_{L1}, i_{L2} and i_{L3} are shown in Fig. 11. Peaks are cancelled each other based on the proposed cancellation technique in Sec. 2.3. The voltage sharing results of the proposed interleaved series configuration, which also take into consideration the voltage drop of the circuit devices, are shown in Fig. 12. The ratio of voltage sharing is satisfactorily matched in the MPP power ratio 1:2:2, as discussed in Sec. 2.5. The enlarged voltages of MICs are shown in Fig. 13, which satisfactorily reduces the overall voltage-ripple in the dc-bus side by using the proposed voltage-ripple cancellation technique.

Experiments are firstly carried out by V–I power supply with boost-MICSs in Sec. 3.1. The results validate that the proposed interleaving method can track the specific current and voltage changes successfully. Then, the implementations move to the PV system under steady-state and transient conditions, as shown in Sec. 3.2.

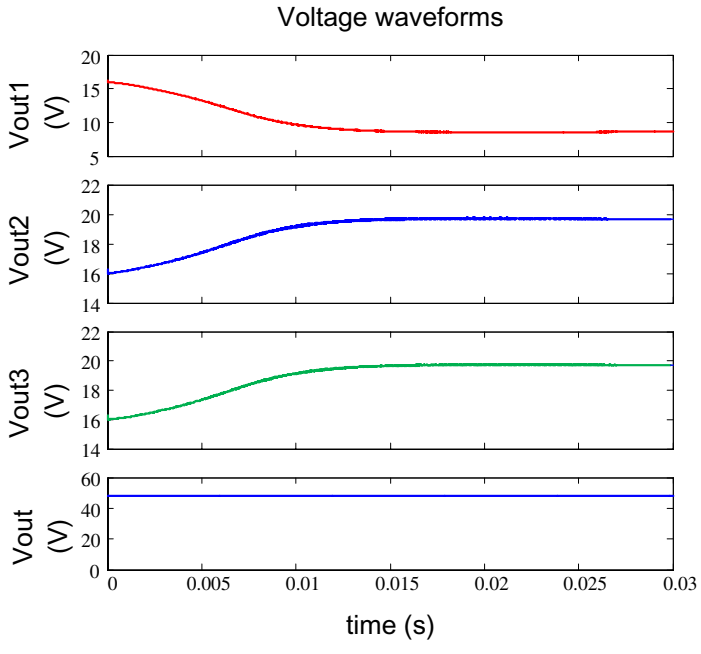

Fig. 12. Key waveforms: V_{out1}, V_{out2}, V_{out3} and V_{out} (color online).

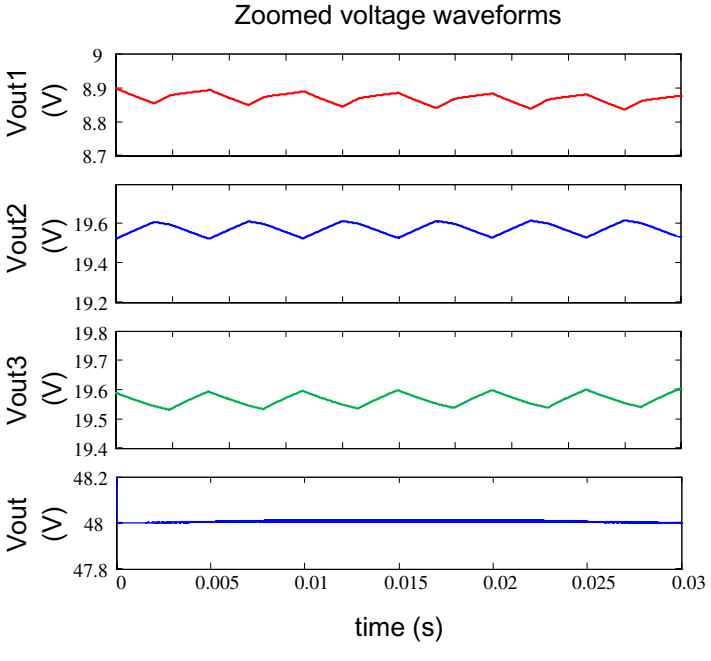

Fig. 13. Enlarged voltage waveforms V_{out1}, V_{out2}, V_{out3} and V_{out} (color online).

3.1. *V–I power supply tests*

Experiments are carried out by two voltage interleaved boost-MICs. Two sources are implemented with the same values of the duty cycles $d_1 = d_2 = 0.5$ and $V_{in1} = 2.05\,\text{V}$, $I_{in1} = 0.2\,\text{A}$, $V_{in2} = 1.38\,\text{V}$ and $I_{in2} = 0.2\,\text{A}$. As can be seen in Fig. 14, the output voltage V_{out2} is successfully shifted to cancel the peak-ripples of V_{out1}, by applying the proposed voltage-ripple cancellation technique. Since the output voltage V_{out} is the sum of V_{out1} and V_{out2}, the ripples from both MICs are cancelled successfully.

The transient and step-change tests are also implemented by a current PI-controller applied to the input source. The reference current is varied initially from 0.2 A to 0.3 A.

Then a step change occurs from 0.3 A to 0.2 A, after which the reference gradually increases from 0.2 A to 0.3 A. As shown in Fig. 15, the ripples of V_{out} are satisfactorily reduced. Compared with the conventional method,[20] which has a duty cycle updated in four switching periods, the proposed method is able to update control duty cycles within one switching period satisfactorily.

Transit tests are implemented by:

(1) d_1 changes from 0.2 to 0.7 and d_2 changes from 0.2 to 0.4,
(2) d_1 decreases gradually from 0.7 to 0.2 and d_2 increases gradually from 0.4 to 0.8, and the experiment results are shown in Figs. 16 and 17, respectively. The switching gate signals are updated immediately within the same switching period.

3.2. *PV interleaving tests*

Two PV panels (bp solar-SX10M) are used for the proposed interleaving method of MPPT tests. The popular P&O MPPT algorithm is used due to its ease of

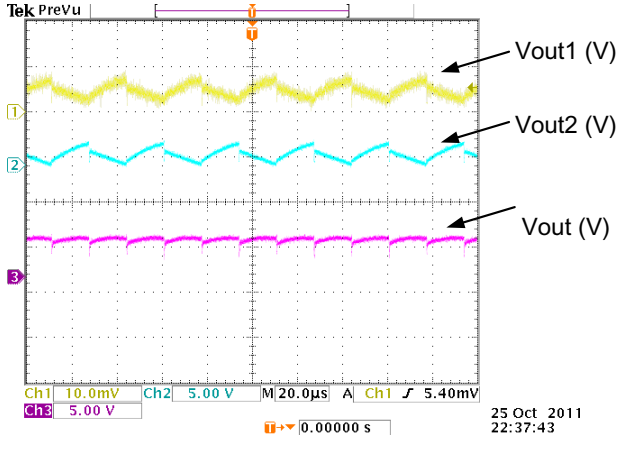

Fig. 14. MIC output voltages V_{out1}, V_{out2} and V_{out} (color online).

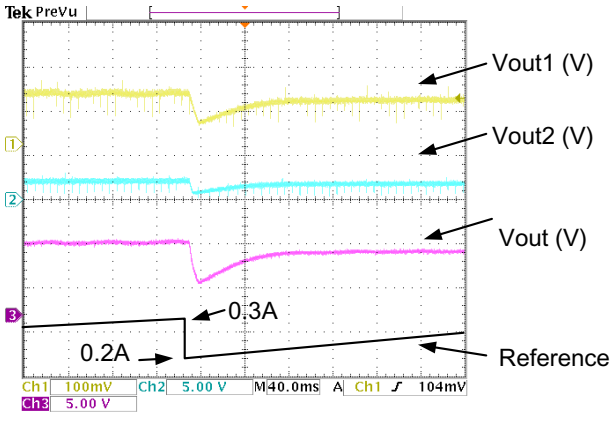

Fig. 15. MIC output voltages V_{out1}, V_{out2} and overall voltage V_{out} (color online).

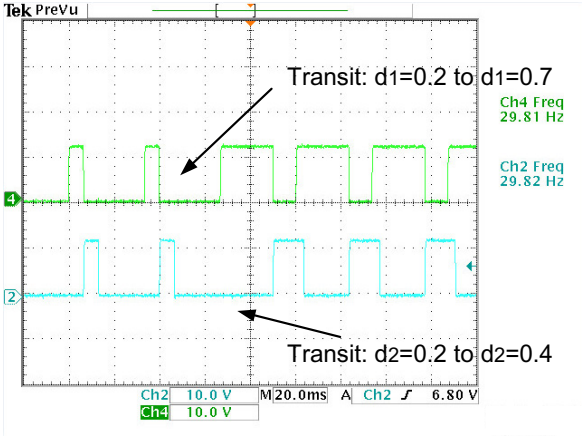

Fig. 16. Gate signals of two converters in transit test 1 (color online).

implementation. It is well known that the perturbation moves PV power operating point toward the MPP, however, there are still some limitations, for example oscillations around MPP in steady-state operation, slow response speed and low-performance under rapidly changing atmospheric conditions. The improved P&O algorithms to accommodate those limitations have been well documented literatures.[46,47] The problem of oscillations around the MPP can be solved by using variable perturbation size that gets smaller towards the MPP as shown in literatures.[46,47] The other example to solve the problem is discussed in the paper,[48] the addition of a "waiting" function is used to reduce the oscillation at MPP in the steady-state for constant irradiance conditions. However, the tracking speed also

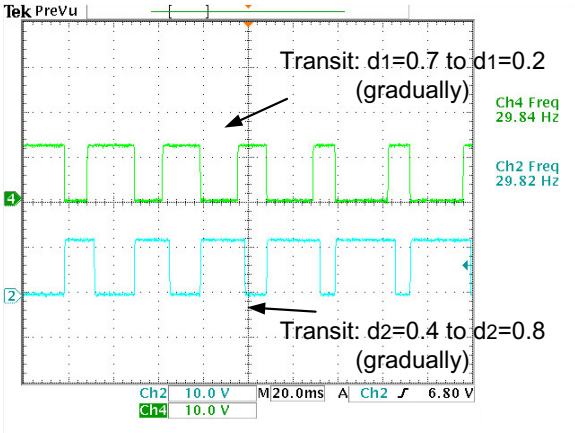

Fig. 17. Gate signals of two converters in transit test 2 (color online).

reduces, which makes the MPPT slower to respond to changing atmospheric conditions. Other technique for improving P&O MPPT performances can be found in paper.[49] In addition, however, the investigation of limitations to different MPPT algorithms, i.e., Incremental Conductance (INC),[50] Constant Voltage (CV),[51] etc. is beyond the scope of this paper. In this paper, the P&Q algorithm is only considered as an example for testing.

Since the experiment setup is based on the interleaving circuit, as explained in Sec. 2.4, which have been embedded into the infrastructure, the following test results are obtained as the interleaved results in both steady-state and transit conditions for

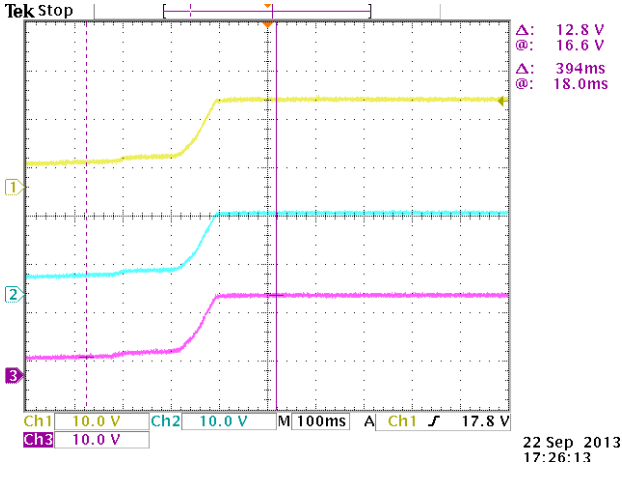

Fig. 18. The transit and steady-state implementation (color online).

voltage ripple reduction. Requirements to the proposed interleaving method can be summarized as follows:

(1) the PV MICs are series-connect,
(2) more than one controllers might be needed depending on
   – the number of MICs in series, and
   – the number of MICs that one controller can accommodate,
(3) interleaving circuit, as explained in Sec. 2.1.4, is needed to shift the switching gate signals for MICs.

As shown in Fig. 18, the two PV panels are tested in transit and steady-state conditions. The PV transit tests show the panels working from shading to steady-state with MPPT algorithm. The proposed interleaving method responses rapidly in transit condition and stably in steady-state condition.

4. Discussion

Due to the fast response feature of the proposed interleaving technique, the converter duty cycle can be updated immediately within the same switching period without any delay or sluggishness, as shown in Figs. 16 and 17. In this paper, a two-input test is satisfactorily implemented in steady-state and transit tests. For the multiple input tests that contain more than two PV sources are addressed in Simulink/Matlab in Sec. 3, however the experimental test just simply repeats and extends the experiment setup from 2 to n MICs in series with the same configurations, which is of a scope beyond this paper. It is in the nature of the series-connect scheme that the fault of one MIC will lead to the string fault, however the proposed method is capable of accommodating the failures of the PV modules. Other interesting applications of the proposed interleaving technique are that they can be integrated into ISOP, ISOS implementations with fast response and reduced voltage ripples in a MIC string. In addition, other research fields, i.e., efficiency gain, output capacitor size-reducing, will be investigated in the future papers and will also extend to parallel-connect configurations.

The proposed interleaving method is investigated based on the scheme PV–converter–dc load. It is clear that the dc load capacitor is not necessary to be large to smooth the dc-load voltage due to the reduced voltage ripples. However, if further considering the scheme of this paper to grid-connect configuration, it should be noted that the inverter voltage oscillations can be transferred to the PV voltage degrading the MPPT efficiency.[49] Therefore, the size of bulk capacitance will mainly depends on the PV isolation from the bulk voltage. The possible solution has been addressed in Ref. 52 by a PV voltage regulator in order to reject (100/120 Hz) disturbances coming from the grid-connected inverter. The analysis of inverter-voltage influence on DMPPT can be found in Ref. 31.

5. Conclusion

The MICs with series connected output is considered in this paper. It is easy to obtain a high dc-link voltage for multiple stage PV system, however the MIC switching ripple of the dc-link voltage also increases as the number of modules increases. An interleaving technique for voltage-ripple cancellation is proposed. The analysis is based on boost MICs with system level investigations. The proposed technique is suitable for many voltage sources in series connection working with different voltage levels and different duty cycles. Satisfactory simulation and experiment results validate that the proposed technique works properly in steady-state, transient and step-change conditions and a few applications for the proposed technique is also suggested with fast response and reduced voltage ripples of MIC strings.

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