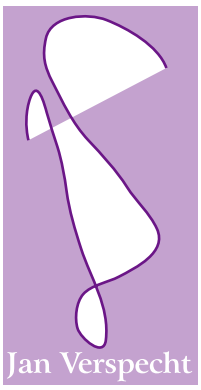

Jan Verspecht bvba

Gertrudeveld 15
1840 Steenhuffel
Belgium

email: contact@janverspecht.com
web: http://www.janverspecht.com

Measurement and Control of Current/Voltage Waveforms of Microwave Transistors Using a Harmonic Load-Pull System for the Optimum Design of High Efficiency Power Amplifiers

D. Barataud, F. Blache, A. Mallet, P. P. Bouysse, J.-M. Nebus,
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Denis Barataud, Fabrice Blache, Alain Mallet, P. Philippe Bouysse, Jean-Michel Nebus, Jean Pierre Villotte, Juan Obregon, Jan Verspecht, *Member, IEEE,* and Philippe Auxemery

***Abstract*—One of the most important requirements that RF and microwave power amplifiers designed for radiocommunication systems must meet is an optimum power added efficiency (PAE) or an optimal combination of PAE and linearity. A harmonic active load–pull system which allows the control of the first three harmonic frequencies of the signal coming out of the transistor under test is a very useful tool to aid in designing optimized power amplifiers. In this paper, we present an active load–pull system coupled to a vectorial "nonlinear network" analyzer. For the first time, optimized current/voltage waveforms for maximum PAE of microwave field effect transistors (FET's) have been measured. They confirm the theory on high efficiency microwave power amplifiers. The proposed load–pull setup is based on the use of three separated active loops to synthesize load impedances at harmonics. The measurement of absolute complex power waves is performed with a broadband data acquisition unit. A specific phase calibration of the set-up allows the determination of the phase relationships between harmonic components. Therefore, voltage and current waveforms can be extracted. The measurement results of a 600 gate periphery GaAs FET (Thomson Foundry) exhibiting a PAE of 84% at 1.8 GHz are given. Such results were obtained by optimizing the load impedances at the first three harmonic components of the signal coming out of the transistor. Optimum conditions correspond to a class F operation mode of the FET (i.e., square wave output voltage and pulse shaped output current). A comparison between measured and simulated current/voltage waveforms is also presented.**

***Index Terms*— Active loop technique, high-efficiency power amplifiers, load–pull/source–pull, microwave and RF transistors, time–domain characterization, vectorial nonlinear network analyzer, voltage/current waveforms.**

I. Introduction

DUE to the expansion of mobile communications systems, the need for high efficiency microwave power amplifiers has emerged. Future generations of mobile telephones require very small size batteries. As a consequence, power amplifiers, which are the most critical element for the power

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D. Barataud, F. Blache, A. Mallet, P. Bouysse, J. M. Nebus, J. P. Villotte, J. Obregon are with IRCOM, University of Limoges, Limoges 87060, France (e-mail: banc@ircom.unilim.fr).

J. Verspecht is with Hewlett-Packard, Brussels, Belgium.

P. Auxemery is with Thomson-TCS, Orsay, France.

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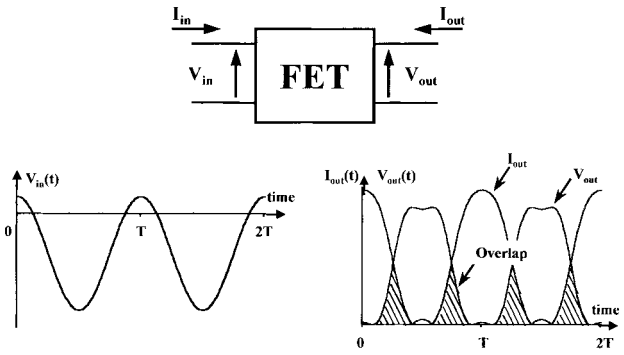


Fig. 1. Class F operation of FETs: voltage/current waveforms.

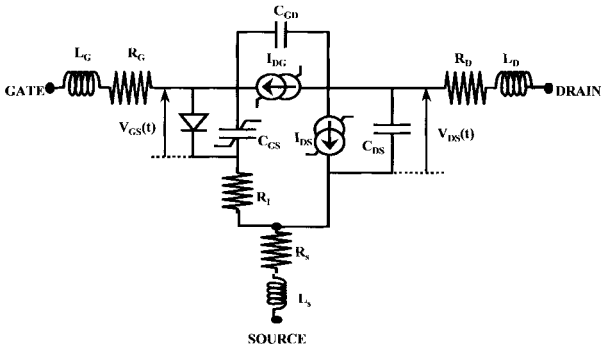


Fig. 2. Nonlinear equivalent circuit of FET.

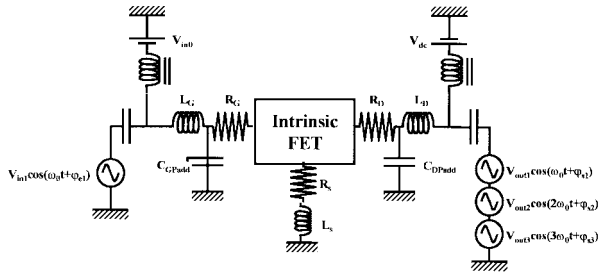


Fig. 3. Principle of the "substitute generator technique."

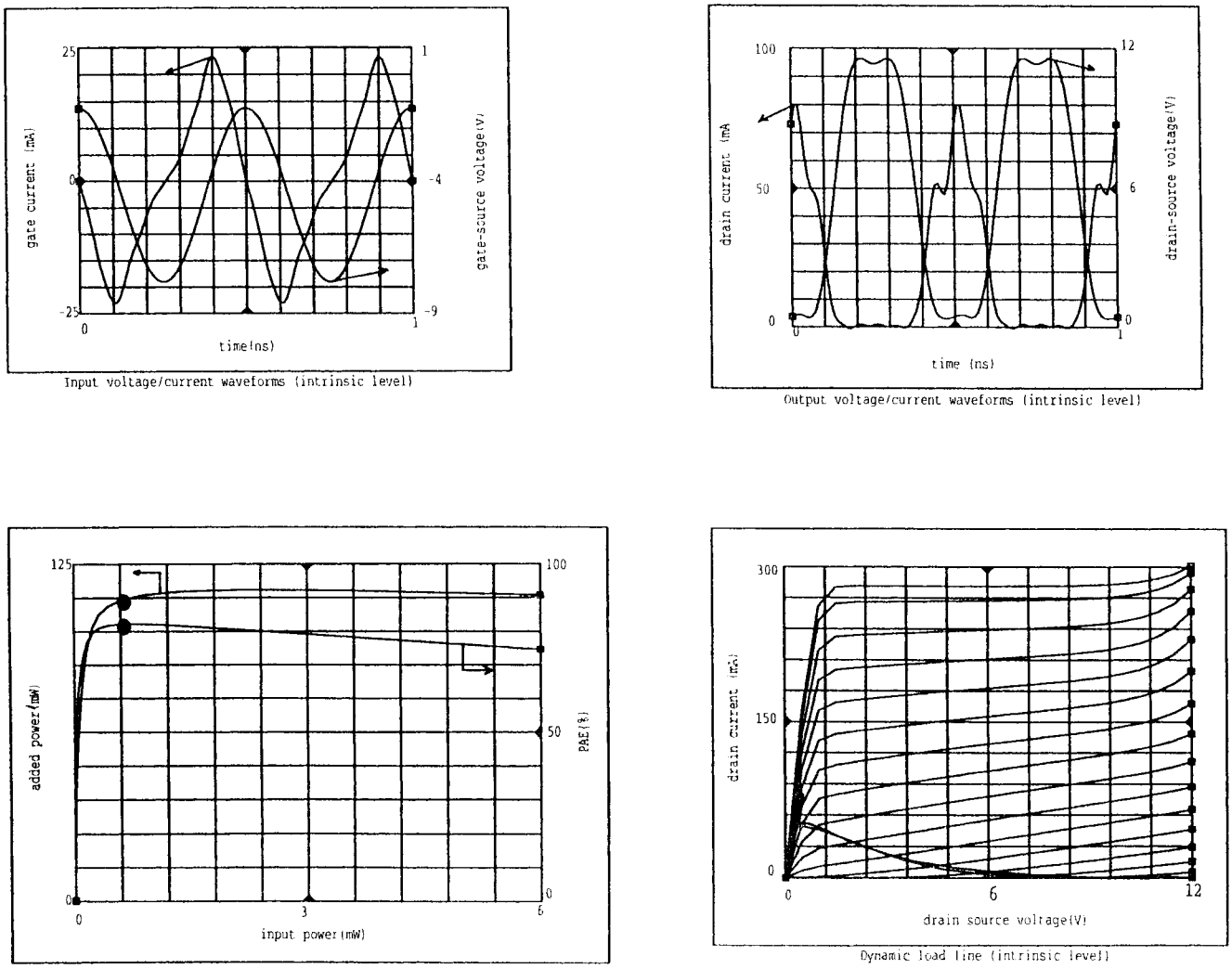


Fig. 4. Simulated time domain waveforms at the intrinsic level.

dissipation budget, must be able to yield high efficiency at very low bias voltages. To optimize the operating conditions of semiconductor devices (for example FET's and HBT's which are expected to be used in such applications) a very quick and accurate optimization tool is increasingly necessary. A harmonic load–pull system coupled to a fully and accurately calibrated vectorial "nonlinear network" analyzer (VNNA) reveals to be very attractive because optimum operating conditions of the device under test (DUT) can be easily, quickly and methodically obtained as explained in this paper. The proposed measurement system can be viewed as a temporal load–pull setup because it allows the control and measurement of current/voltage waveforms at both ports of the DUT. Although measurements of microwave time domain waveforms in a 50 Ω environment have already been performed and reported [1]–[5] the optimization of voltage/current waveforms for maximum added power or PAE by monitoring the load impedances at the first three harmonics generated by the DUT has never been reported to our knowledge.

II. Preliminary Considerations on High Efficiency Class F Operation of Microwave FETs

It is necessary to know current/voltage waveforms at both ports of any transistor to understand the operation. Time domain waveforms allow circuit designers to have an accurate insight into the operating mode of transistors. Furthermore, voltage/current waveforms provide a very good understanding and visualization of the main nonlinear phenomena (like generation of harmonics or saturation mechanisms).

It is now well accepted that FET's exhibit their best performances in terms of PAE at L-band when they are operated under class F conditions [6]. Theoretically speaking, a transistor is operated under class F conditions if the input voltage is purely sinusoidal, the output voltage is a quasisquare wave signal and the output current is pulse shaped. The PAE of the transistor is optimized if the overlap between the output current and the output voltage is minimized (Fig. 1). As a consequence, the power dissipated by the device is minimized.

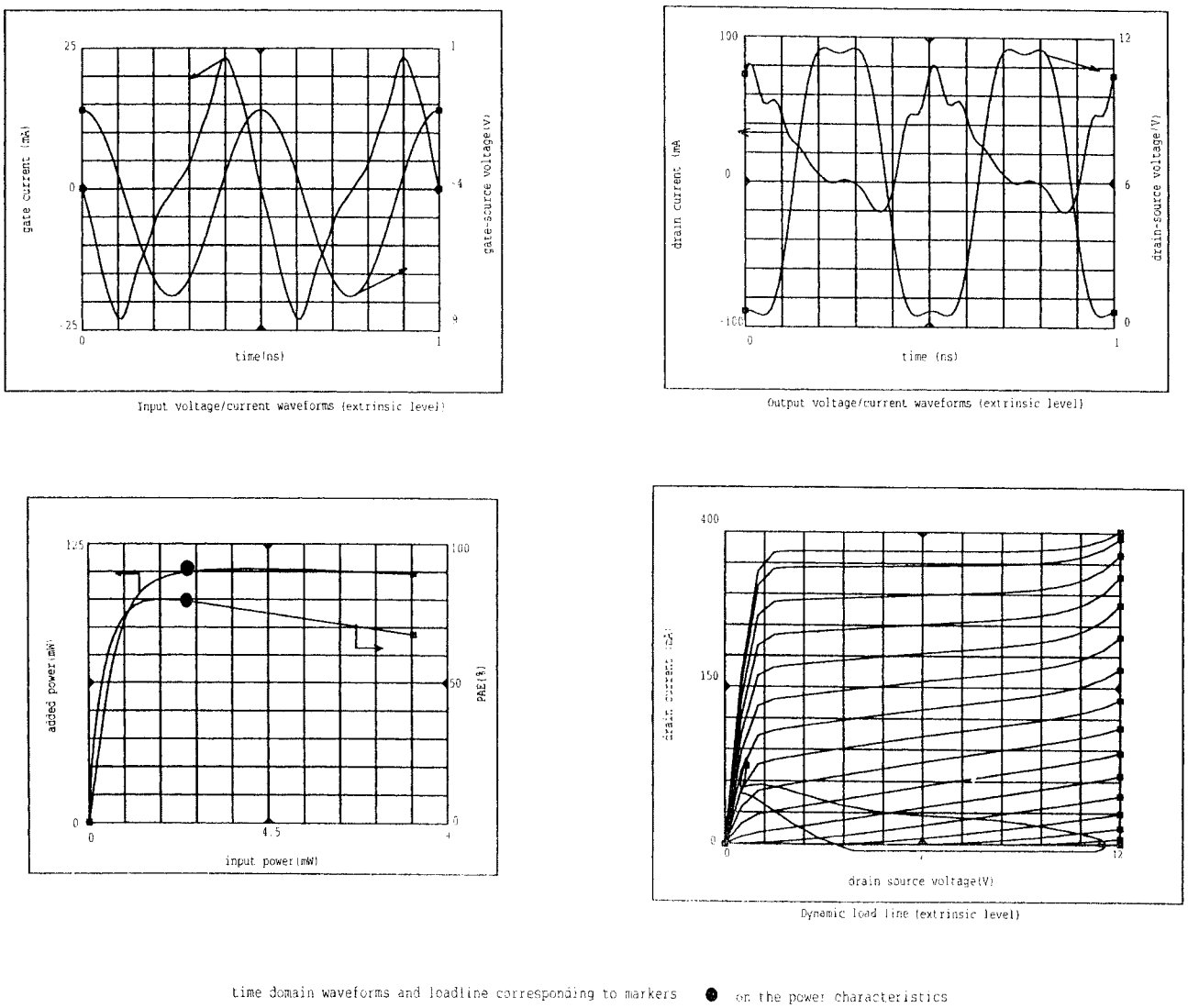


Fig. 5. Simulated time domain waveforms at the extrinsic level.

It is easy to perform simulations to get the optimal combination of current and voltages depicted in Fig. 1 [7]. Nevertheless, the control and optimization of the appropriate waveforms by experimentation is very difficult and requires a sophisticated and fully calibrated setup (part II of the paper). The originality of the work reported in this paper lies in the fact that the optimization of waveforms corresponding to a class F operation of FET's has been reached by experimentation.

The simulation and the optimization of PAE of transistors operated under class F conditions can be performed in a straightforward manner by using any commercially available nonlinear software and applying what we call the "substitute generator technique" [8].

First, a nonlinear electrical model of FET must be extracted (for example, pulsed I/V and pulsed S parameter measurements can be performed for that purpose [9]) (Fig. 2). Then, generators are connected to both ports of the transistor (Fig. 3). The input generator supplies a purely sinusoidal voltage while the output generator supplies a quasisquare waveform signal.

Taking into account only three harmonic components, it has been demonstrated [10] that for a fixed drain bias voltage $V_{\rm dc}$, the optimum voltage $V_{\rm out}(t)$ necessary to maximize the ratio $V_{\rm out1}/V_{\rm dc}$ is given by the expression

$$V_{\rm out}(t) = V_{\rm dc}\left(1 - \frac{2}{\sqrt{3}} - \cos(\omega_0 t) + \frac{2}{3\sqrt{3}}\cos(3\omega_0 t)\right) \tag{1}$$

where $V_{\rm out1} = (2V_{\rm dc}/\sqrt{3})$ represents the magnitude of the fundamental component of $V_{\rm out}(t)$.

If $V_{\rm out1}/V_{\rm dc}$ is maximized and equal to $2/\sqrt{3}$, PAE will be optimized.

Probes are also connected to the transistor in order to determine the associated currents. The equivalent optimum load impedances of the embedding circuit are determined by nonlinear analysis. They are given by

$$Z_{{\rm out}n} = -\left(\frac{\tilde{V}_{{\rm out}n}}{\tilde{I}_{{\rm out}n}}\right) \tag{2}$$

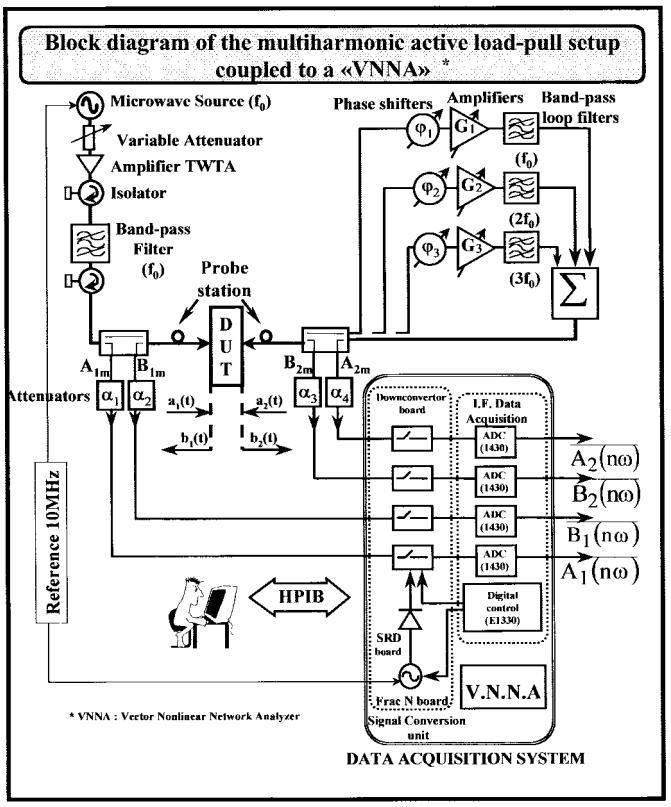


Fig. 6. Block diagram of a VNNA coupled to an harmonic load–pull setup.

where $\tilde{V}_{\text{out}n}$ and $\tilde{I}_{\text{out}n}$ are the complex nth harmonic components of the output voltage and current.

The conditions $\text{Re}[Z_{\text{out}n}] > 0$ must obviously be verified (Re denotes the real part).

Figs. 4 and 5 show respectively the simulated optimum voltage and current waveforms and the associated dynamic load lines at the intrinsic and extrinsic ports of the transistor. An optimum PAE of 80% with a power gain of 17 dB and an output power of 110 mW have been obtained at a drain bias voltage of 6 V.

III. Description of the Time Domain Waveforms Measurement System

For the extraction of time domain waveforms the measurements of the following signals are necessary:

$$a_1(t) = a_{11}\ \cos(\omega_0 t + \varphi_{11}) + a_{12}\ \cos(2\omega_0 t + \varphi_{12}) + \cdots + a_{1n}\ \cos(n\omega_0 t + \varphi_{1n}) \quad (3)$$

$$a_2(t) = a_{21}\ \cos(\omega_0 t + \varphi_{21}) + a_{22}\ \cos(2\omega_0 t + \varphi_{22}) + \cdots + a_{2n}\ \cos(n\omega_0 t + \varphi_{2n}) \quad (4)$$

$$b_1(t) = b_{11}\ \cos(\omega_0 t + \theta_{11}) + b_{12}\ \cos(2\omega_0 t + \theta_{22}) + \cdots + b_{1n}\ \cos(n\omega_0 t + \theta_{1n}) \quad (5)$$

$$b2(t) = b_{21}\ \cos(\omega_0 t + \theta_{21}) + b_{22}\ \cos(2\omega_0 t + \theta_{22}) + \cdots + b_{2n}\ \cos(n\omega_0 t + \theta_{2n}). \quad (6)$$

A conventional vector network analyzer is not sufficient because it can only provide complex power wave ratios at the fundamental and harmonic frequencies

$$\frac{b_{1n}}{a_{1n}}\ e^{j(\theta_{1n}-\varphi_{1n})}, \quad \frac{b_{2n}}{a_{1n}}\ e^{j(\theta_{2n}-\varphi_{1n})}$$
$$\frac{b_{1n}}{a_{2n}}\ e^{j(\theta_{1n}-\varphi_{1n})}, \quad \frac{b_{2n}}{a_{2n}}\ e^{j(\theta_{2n}-\varphi_{2n})}.$$

1) The magnitude of the power waves can be measured by using a selective power meter.
2) The determination of the phase relationships between the harmonic components of the power waves remains the most difficult problem encountered.

Let us assume that φ_{11} is taken as a phase reference, then $(\varphi_{1n}, \varphi_{11}), (\varphi_{2n} - \varphi_{11}), (\varphi_{1n} - \varphi_{11}), (\varphi_{2n} - \varphi_{11})$ must be accurately known in order to determine time domain waveforms $a_1(t), a_2(t), b_1(t), b_2(t)$.

For that, a vectorial "nonlinear network" analyzer, operating up to 40 GHz, and a specific phase calibration procedure are required [10]. A block diagram of the measurement system is sketched in Fig. 6.

A fully synchronized four channel down converter has been built based on sampling technology. Four couplers are used to detect the incident and scattered waves at both ports of the DUT. Attenuators are used to bring the level at the input of the broadband down convertor below -10 dBm. This is necessary to assure linearity of the samplers in the down convertor.

The broadband down converter uses the harmonic mixing principle to convert RF fundamental and harmonics into IF fundamental and harmonics. Four data acquisition modules (ADC converters) with a sampling rate of 10 MHz are used to digitize IF signals. At the output of the down convertor circuit, the useful mixing products at frequencies below 4 MHz represent an image of the input RF spectrum (0.9–40 GHz) [11]. Three active loops are used to synthesize load impedances at the first three harmonics of the signal coming out of the DUT [12].

By the active loop technique, the loads at harmonic frequencies can be independently adjusted by varying both the gain and the phase shift of each loop. At the fundamental frequency f_0, by using the mismatching technique [13], the synthesized impedances are automatically focused in the optimum load impedance area.

At harmonic frequencies ($2f_0$ and $3f_0$), any load-impedances in the Smith chart can be synthesized and it is possible to reach high reflection coefficient to simulate high efficiency operating classes.

Moreover, the measurement of added power, PAE, AM/PM and third order intermodulation versus input power is automatically obtained by sweeping the input power driving the device.

After calibration, the VNNA is able to measure the amplitude and the phase of the harmonic components of the incident and scattered power waves. Systematic amplitude and phase errors due to the measurement channels are taken into account and corrected.

The calibration sequence consists of three main steps:

1) TRL calibration for the correction of complex power wave ratios $(b_{jn}/a_{\text{in}}) = i, j = 1, 2$;

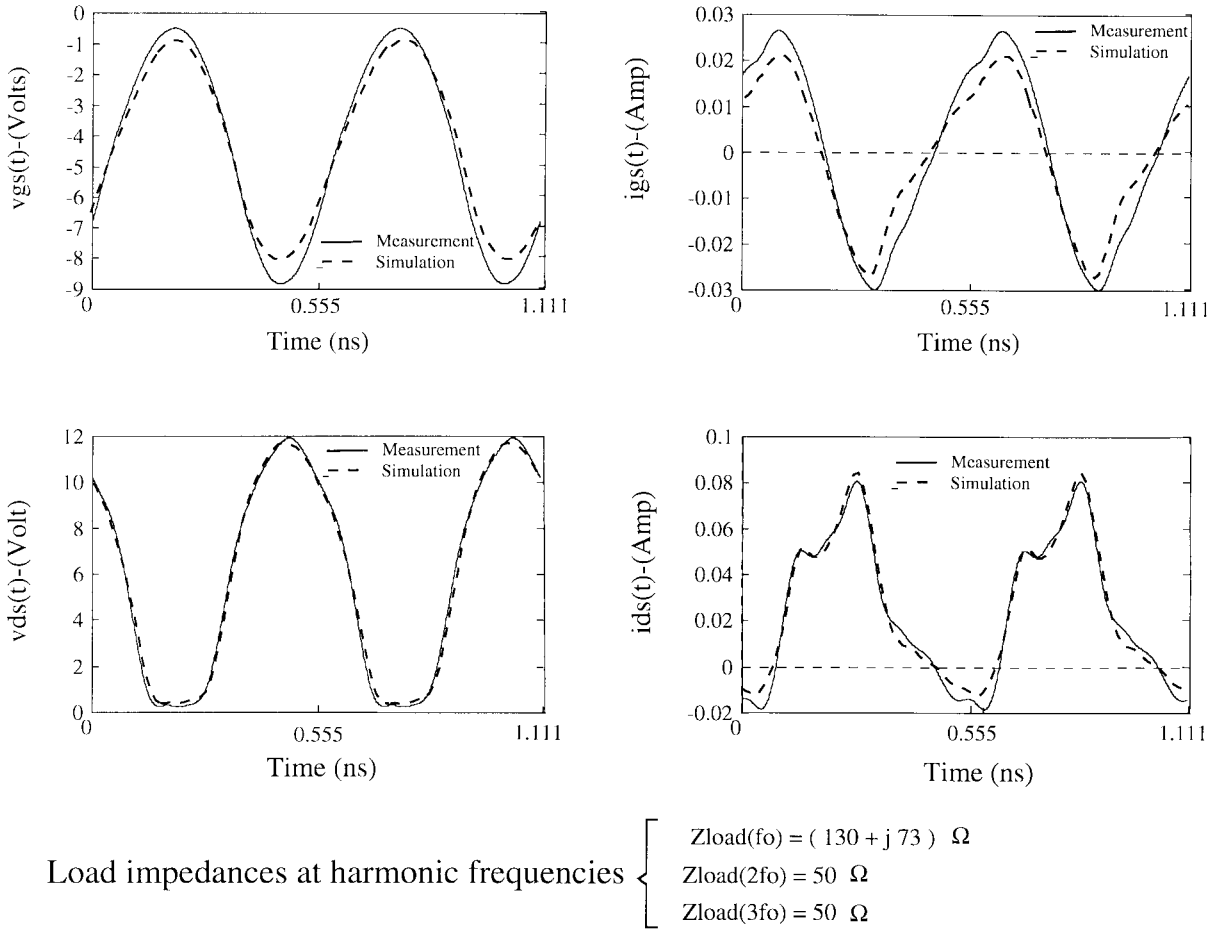


Fig. 7. Measured voltage/current waveforms at a 6 V drain bias voltage (harmonic loads = 50 Ω).

2) absolute power measurements using an accurate power meter, for the determination of $(a_{\mathrm{in}}), (b_{\mathrm{in}})$;
3) phase calibration which is a key point for which a multiharmonic generator (SRD) is used. This generator is used as a reference standard for phase calibration in a similar way as a powermeter is used for the amplitude calibration. Relationships between the phase of harmonics are initially determined using a sampling oscilloscope calibrated using the so-called "nose-to-nose" procedure [14]. The phase calibration allows the determination of the phase of the complex power waves φ_{in} and θ_{in}.

As error corrected complex power waves $\tilde{a}_{1\mathrm{n}}, \tilde{b}_{1n},, \tilde{a}_{2n}, \tilde{b}_{2n}$ are determined, voltage and current waveforms can be extracted:

$$V_{\mathrm{in}}(t) = V_{\mathrm{in0}} + \sum_n V_{\mathrm{in}n} \cos(n\omega_0 t + \varphi_{\mathrm{in}n}) \quad (7)$$

$$V_{\mathrm{out}}(t) = V_{\mathrm{out0}} + \sum_n V_{\mathrm{out}n} \cos(n\omega_0 t + \varphi_{\mathrm{out}n}) \quad (8)$$

$$I_{\mathrm{in}}(t) = I_{\mathrm{in0}} + \sum_n I_{\mathrm{in}n} \cos(n\omega_0 t + \theta_{\mathrm{in}n}) \quad (9)$$

$$I_{\mathrm{out}}(t) = I_{\mathrm{out0}} + \sum_n I_{\mathrm{out}n} \cos(n\omega_0 t + \varphi_{\mathrm{out}n}). \quad (10)$$

$V_{\mathrm{in0}}, V_{\mathrm{out0}}, I_{\mathrm{in0}}, I_{\mathrm{out0}}$ are measured using programmable dc power supplies.

$$V_{\mathrm{in}n} e^{j\varphi_{\mathrm{in}n}} = \sqrt{Z_0}(a_{1n} + b_{1n}) \quad (11)$$

$$V_{\mathrm{out}n} e^{j\varphi_{\mathrm{out}n}} = \sqrt{Z_0}(a_{2n} + b_{2n}) \quad (12)$$

$$I_{\mathrm{in}n} e^{j\theta_{\mathrm{in}n}} = \frac{1}{\sqrt{Z_0}} (a_{1n} - b_{1n}) \quad (13)$$

$$I_{\mathrm{out}n} e^{j\theta_{\mathrm{out}n}} = \frac{1}{\sqrt{Z_0}} (a_{2n} - b_{2n}) \quad (14)$$

where Z_0 is equal to 50 Ω.

By using the active loop principle, optimum load impedances at harmonics can be accurately and methodically tuned in order to maximize the PAE of the DUT. The key point of the whole system is that load impedances at harmonics are fully independent of the behavior of the transistor and the power levels. Moreover, the tuning of a loop at one frequency is independent of the loops at other frequencies. This makes the optimization process of load impedances more easier and more efficient.

IV. Measurement Results

On-wafer measurements of a 600 μm gate periphery GaAs MESFET (Thomson Foundry) have been performed using

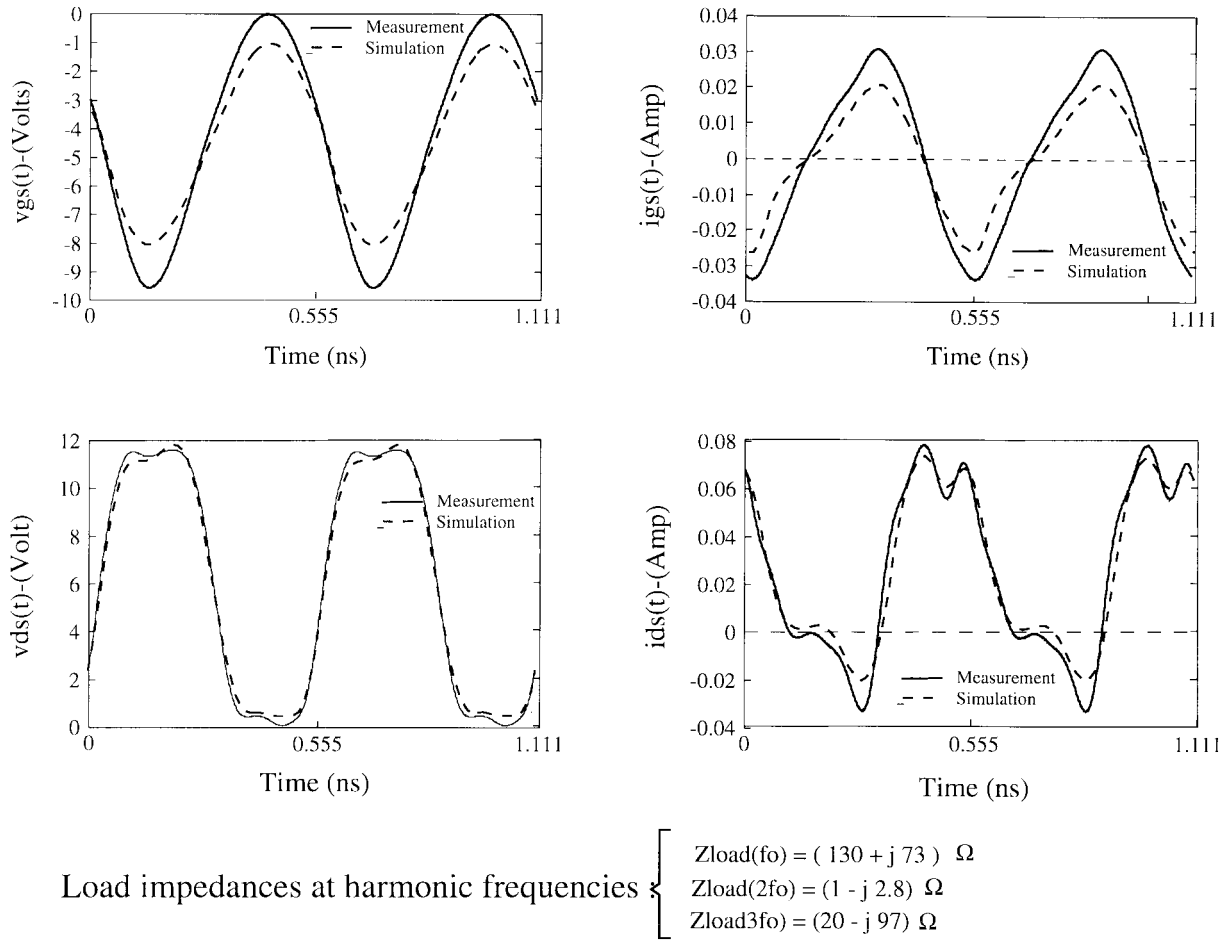
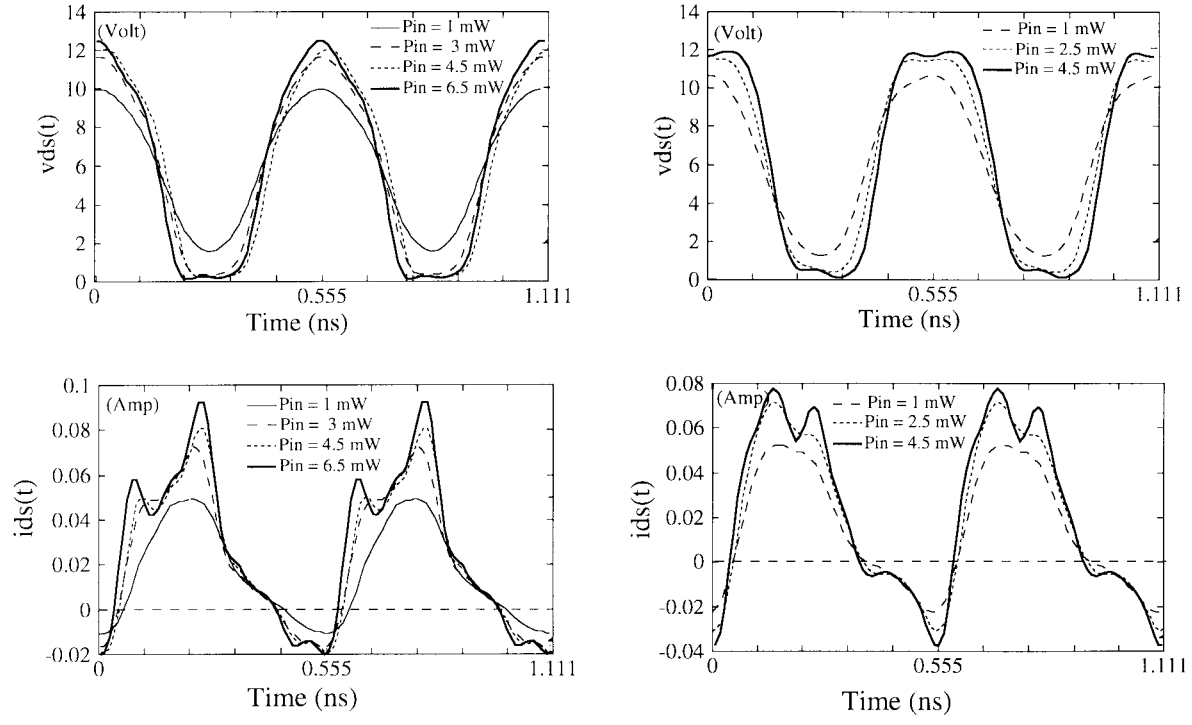


Fig. 8. Measured voltage/current waveforms at a 6 V drain bias voltage (optimized harmonic loads).



(a) (b)

Fig. 9. Measured voltage/current waveforms as a function of the input power. (a) Optimized load at the fundamental and harmonic loads are 50 Ω and (b) optimized load at the fundamental and harmonics.

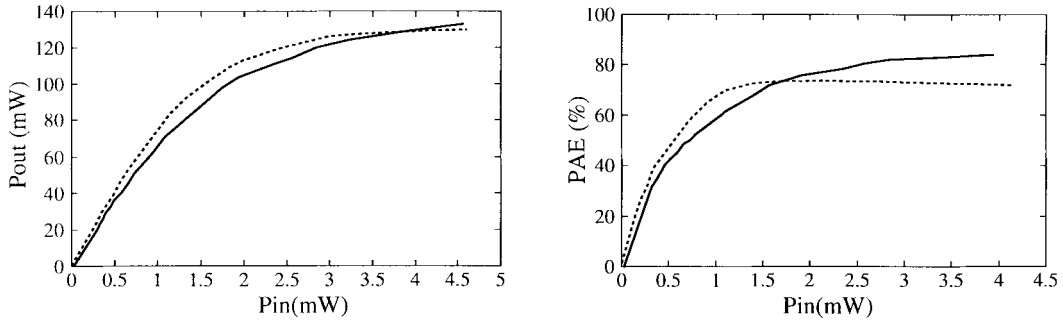


Fig. 10. Measured and simulated power characteristics as a function of the input power.

a probe station. Fig. 7 shows measured and simulated voltage/current waveforms when the transistor is biased at a dc drain voltage of 6 V and when the harmonic loads are 50 Ω. In this case, the MESFET exhibits an output power of 130 mW, a power gain of 14 dB and a power added efficiency of 75%.

Fig. 8 shows the same kind of results obtained when harmonic loads are optimized. The measured waveforms validate the theoretical optimal combination of output current and voltage required for a class F operation mode. In that case, an optimum PAE of 84%, a power gain of 14.6 dB and an output power of 130 mW were measured.

Fig. 9 shows measured voltage/current waveforms as a function of the input power in both cases. (Fig. 9(a): harmonics loads $= 50\ \Omega$; Fig. 9(b): optimized harmonic loads.)

Fig. 10 shows power characteristics as a function of the input power in the case of an optimized class F operation mode. A good agreement between simulated and measured curves is observed.

It has been clearly demonstrated by experimentation that a quasisquare drain voltage yields the optimal PAE. Time domain waveforms are very similar at the intrinsic and the extrinsic level of the transistor because it operates at low microwave frequencies (1.8 GHz).

V. Conclusion

The analysis and the measurement of time domain waveforms at transistor ports have proved to be very efficient and well-suited for the optimization of high efficiency microwave amplifiers.

Moreover, it would be possible to optimize class E amplifiers using the same method as described in this paper. Generally speaking, the optimization of source impedances at harmonics for high efficiency operation can be implemented.

The proposed novel measurement system is shown to be also an important and valuable tool to aid in the modeling of semiconductor devices. It is expected to provide valuable information for the validation of nonlinear electrical models of FET's in the ohmic region where capacitors C_{gs} and C_{gd} are strongly nonlinear functions of both V_{gs} and V_{ds}.

The multiharmonic load–pull concept based on active loops can be extended to the experimental study and optimization of frequency multipliers or dividers. It can also be applied to an extensive analysis of intermodulation in transistors (two tone characterization (IM3) or noise power ratio (NPR) measurements).

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Denis Barataud was born in Saint-Junien, France, in 1970. He graduated from Ecole Nationale Supérieure de Télécommunications de Bretagne in 1994. He received the Ph.D. degree in electronics from the University of Limoges, Limoges, France, in 1998.

He joined the Microwave Laboratory of the CNES of Toulouse, France, in 1998. Currently, he's working on NPR measurements. His main research interest is the characterization of nonlinear devices.

Fabrice Blache was born in Neuvicentier, France, in 1968. He received the Ph.D. degree in electronics from the University of Limoges, Limoges, France, in 1995.

Currently he works on the optimization of power efficiency in SSPA's.

Alain Mallet was born in Limoges, France, in 1971. He received the Ph.D. degree in electronics from the University of Limoges in 1996.

His research interests include active microwave and millimeter-wave circuit design, HBT modeling, and characterization.

Philippe Bouysse was born in Aurillac, France, in 1965. He received the Ph.D. degree in communication engineering from the University of Limoges, France, in 1992.

Since 1992, he has been with the Microwave Laboratory of the University of Limoges. His main research interest is the optimization of power-added efficiency and intermodulation products in SSPA's.

Jean-Michel Nebus was born in Bourganeuf, France, in 1963. He received the Ph.D. degree in communication engineering from the University of Limoges, Limoges, France, in 1988.

From 1988 to 1990, he was an Engineer at ALCATEL ESPACE, France, where he was involved in the TELECOM 2 satellite payload development. In 1990, he rejoined the University of Limoges as a Teacher and Researcher in microwave circuits.

Jean Pierre Villotte was born in Abjat, France, in 1946. He received the "Doctorat de troisième cycle" from the from the University of Limoges, Limoges, France, in 1978.

From 1971 to 1985, his research interests were the applications of the finite element-method in microwave transmission lines. Since 1985, his main area of interest has been the experimental characterization of nonlinear devices and applications to the optimization of telecommunication power amplifiers.

Juan Obregon received the Ph.D. degree from the University of Limoges, Limoges, France.

He was appointed Professor in 1981. He has held a number of positions in the microwave industry with Thomson CSF and RTC France. His fields of interest are the modeling, simulation, and design of nonlinear circuits and subsystems.

Dr. Obregon was awarded the European Microwave Prize in 1985 for a work on millimeter-wave DROS.

Jan Verspecht (M'94) was born in 1967 in Merchtem, Belgium. He received the Eng. and Ph.D. degrees from the University of Brussels (VUB), Brussels, Belgium, in 1990 and 1995, respectively.

As a member of the Hewlett-Packard Network Measurement and Description Group, Brussels, he is currently working on advanced calibration, measuring and modeling methods for nonlinear microwave devices.

Philippe Auxemery was born in Limoges, France, in 1963. He received the Ph.D. degree in electronics from the University of Limoges in 1990.

Since 1990, he has been an Engineer at United Monolithic Semiconductor, Orsay, France, where he's been working on the design of microwave power amplifiers.