Electronics for Ultrasonic Imaging System

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***Abstract*—Design of ultrasonic imaging system is presented. System has a modular structure with main acquisition and front end electronics separated in order to have minimal path for host PC connectivity and shortest path to ultrasonic transducer. Such acquisition modules placement allows reducing the induced EMI and increasing the flexibility of the system. Positioning module is also separate and allows various scanning equipment configurations. Evaluation of excitation and reception electronics parameters is presented. Essential measurement procedures outlined. Signal digitization parameters (sampling frequency, clock jitter and quantisation) were chosen to balance time of flight estimation random errors versus interpolation bias errors.**

***Index Terms*—Ultrasonic imaging, ultrasound electronics, data acquisition, signal sampling.**

I. INTRODUCTION

Thanks to the direct interaction with material structure ultrasonic probing can extract the mechanical properties related information which later can be used in measurement or imaging. Ultrasonic imaging is used in non-destructive testing (NDT) and evaluation (NDE) [1]–[3]. Coating or layers thickness can be measured [4], mechanical properties evaluation [5], non-contact temperature visualization [6], surface profiling [7], medical diagnostic, tissue temperature or elasticity imaging [8]. Ultrasonic system can be small [9], [10] equipment is safe and easy in exploitation. Quality of the image obtained is defined by the imaging method used, ultrasonic transducer and signal acquisition electronics. If system is dedicated for particular task, then it is important to keep the size and the price of the electronics down. In such case functionality and data quality are sacrificed. System flexibility and acquisition quality is essential in ultrasonic data acquisition for research purposes.

The goal of this paper is to present the design and development of the electronics of the ultrasonic imaging system. Ultrasonic data acquisition system has to carry several tasks: provide the excitation signal for ultrasonic transducer; position the transducer; receive and process the received signal; transfer data to or from PC. Modular construction was suggested in order to ensure the flexibility of the system. Parameters of the main units were selected to match the expected performance and balanced in a sense of power consumption, size and price. Design considerations and parameters evaluation procedures are presented.

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II. SYSTEM STRUCTURE

Data acquisition system for ultrasonic imaging has been designed (Fig. 1). System is modular: i) front-end module; ii) main acquisition module; and iii) positioning module.

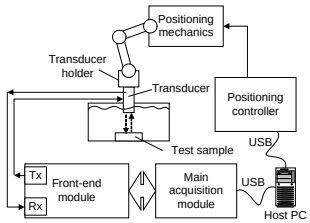

Fig. 1. General system structure showing its modular construction.

Front-end module (Fig. 2) is placed in close proximity to ultrasonic transducer in order to reduce the electromagnetic interference. This module contains high voltage pulser (Tx), programmable high voltage power source and low noise preamplifier with high voltage protection circuits (Rx).

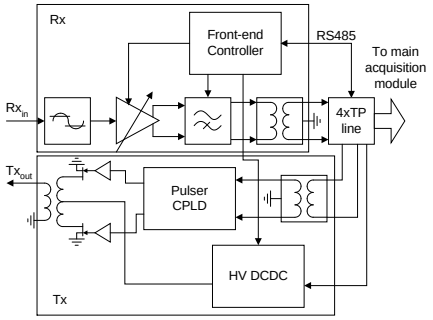

Fig. 2. Analog front-end module structure.

Main acquisition module (Fig. 3) is located near the host PC. It contains the excitation signal transmission unit (Tx) and the signal reception unit (Rx). Transmission unit contains buffer drivers which route the driving signals to excitation part of the front-end module. Driving signals are derived from RAM organised in main FPGA. Reception unit is responsible for additional gain of the incoming signal, analog filtering, analog-to-digit conversion (ADC), digital signal processing and data transfer (Rx). FPGA is used for ADC data storage management, serial communication with front-end module, communication with GPIO part of the USB controller and synchronisation.

Positioning module contains the controller, motor drivers and positioning mechanics. Controller is capable of steering of up to four motor controllers. Several options of the positioning mechanics can be used: i) universal 3D positioning scanner or ii) dedicated translation stage (Fig. 4).

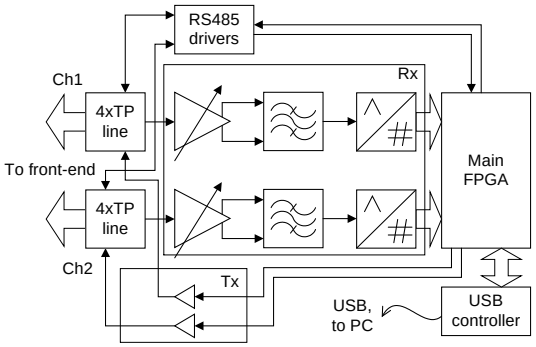

Fig. 3. Main acquisition module structure.

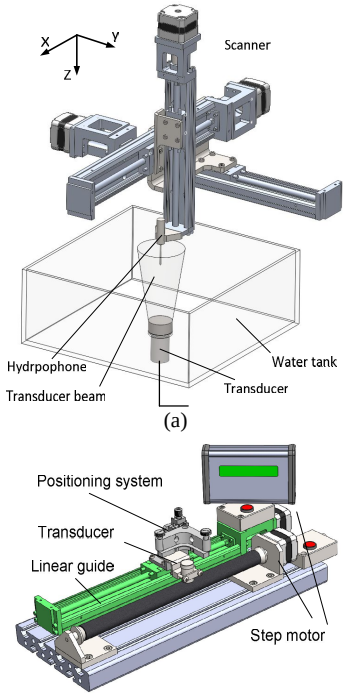

Fig. 4. Positioning module options: 3D scanner (a) or sleeve (b).

All modules are replaceable in order to attain different functionality. E.g. analog front-end can be replaced by multichannel module, allowing phased array imaging or fast electronic scan.

Design considerations and parameter measurements of the aforementioned units are presented below.

III. Excitation Electronics

As can be seen from Fig.1 the ultrasonic transducer is main device connecting the electrical and acoustical parts of the system. It is used to convert the electrical power into mechanical energy and vice versa [11]. Mechanical stress propagating in the test material is interacting with material structure in the propagation path and in case of mechanical impedance mismatch is reflected back. Flaws in the material can be located by analysing the reflected signals. The most common transducer types represent the capacitive load to the excitation electronics. Therefore main task of the excitation circuit is a fast charge and discharge of the capacitive load. Most common type excitation signal is a rectangular pulse or step [12], [13].

Usually power MOSFET is used as a power switch thanks to its speed and high current delivery capability [13], [14]. In order to remove the charge from C_0 at the end of excitation pulse additional element is needed to pull the output voltage low. Conventional pulser topology where only one active element and return resistor are used [13] is not suitable here – return resistor draws current during the excitation pulse lowering the overall system efficiency. The most attractive is the totem pole topology [14]–[16]. This topology is using two N-channel MOSFETs. Full voltage swing can be applied here. Problem with such configuration is the delivery of the driving signal to high side switch: floating driver and power supply are needed here. Therefore topology is mainly used for voltage below 100 V [15] or high voltage but low frequency [14]. Using P-channel MOSFET for high side driving is more convenient [16] but performance still suffers since high voltage P-channel MOSFETs are slow.

Another possible topology is the transformer push-pull [17], [18] (Fig. 5). Low side switches can be used here. Summation is accomplished using the transformer.

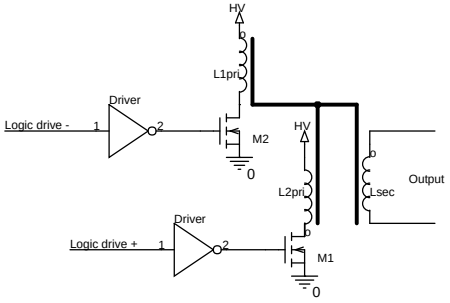

Fig. 5. Pulser output topology: transformer push-pull with two MOSFETs.

Main advantage is the ability to use low side drivers; symmetrical driving conditions for both rising and falling edges; output isolation and possibility to have positive and negative pulses using only one high voltage power supply. Fast switching is possible thanks to optimal driving circuit topography.

A. Pulser Output AC Response Estimation

Output signals were registered by the same acquisition system (Fig. 1). Excitation signal was preloaded into system memory as ten periods long CW burst (Fig. 6).

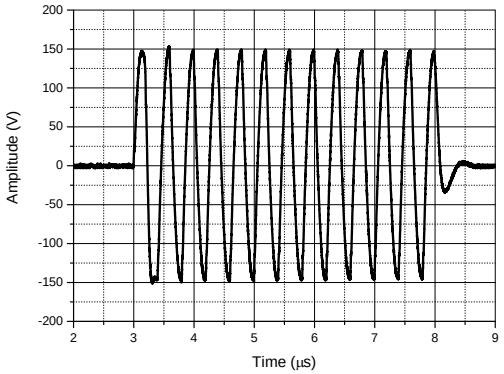

Fig. 6. Pulser output waveform example when used for AC response.

Main harmonic amplitude was extracted using the Sine Wave Correlation (SWC) technique. SWC technique [19] can be treated as partial Fourier transform. Correlation coefficient of the signal sampled version s_n with sine and

cosine functions:

$$\begin{cases} C(f) = \dfrac{2\sum_{n=0}^{N-1}\left[\cos(2\pi f t_n)\times s_n \times w_n\right]}{N|W|_1}, \\ S(f) = \dfrac{2\sum_{n=0}^{N-1}\left[\sin(2\pi f t_n)\times s_n \times w_n\right]}{N|W|_1}, \end{cases} \quad (1)$$

where w_n is a window function, N is record length and $|W|_1$ is a L1 norm of the window function. For output response measurements rectangular window was used: recorded signal was cropped to exactly ten periods of the fundamental frequency. Pulser output signals were recorded using 1:100 divider formed by 5 kΩ and 50 Ω resistors which was also accounted in calculations. Resulting output AC response is presented in Fig. 7.

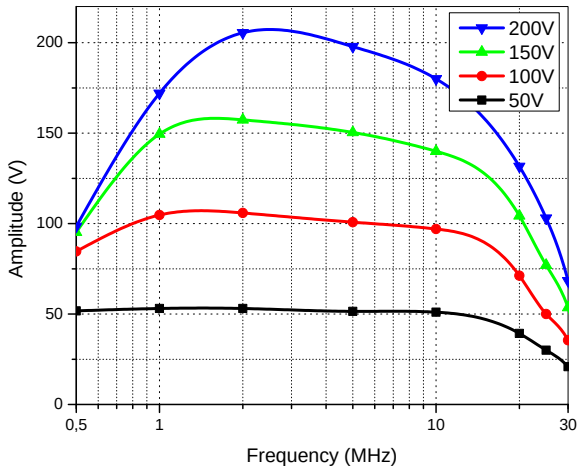

Fig. 7. Pulser output AC response versus voltage swing ±.

It can be seen that excitation up to 25 MHz is achieved. Available bandwidth is reduced with increase of the excitation voltage span.

B. *Pulser Output Impedance Measurement*

Interaction of the pulser output impedance and transducer input impedance will cause the variation of the excitation voltage. In order to keep this voltage constant and be able to predict the efficiency of power delivery to transducer [14] investigation of pulser output impedance Z_o was carried out.

Pulser output impedance Z_o together with the impedance Z_T of the ultrasonic transducer can be used for power delivery efficiency evaluation [14]. It can be assumed that real part of complex power delivered to ultrasonic transducer reflects the power transmitted by transducer (if transducer design is optimal). Then the power delivery to ultrasonic transducer efficiency is

$$\eta = \frac{4\,\mathrm{Re}(Z_o)\,\mathrm{Re}(Z_T)}{|Z_o + Z_T|^2}100\%, \quad (2)$$

Pulser output impedance was measured by taking two output voltages registered at 50 Ω (V_{50}) and 75 Ω (V_{75}) load conditions [19], [20]

$$Z_o = \frac{50\times 75\times(V_{75} - V_{50})}{75\times V_{50} - 50\times V_{75} N_0}, \quad (3)$$

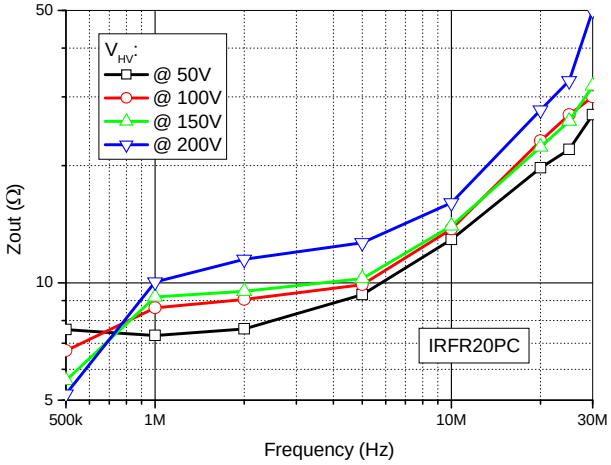

Fig. 8. Pulser output impedance versus frequency.

Complex voltage values were obtained by using the SWC. Results for output impedance magnitude AC response versus output voltage swing are presented in Fig. 8. It can be noted that output impedance magnitude is stable with output voltage and is rising with output frequency (5 Ω to 30 Ω).

C. *Pulser Power Consumption Evaluation*

Pulser is using two switches to save the energy when there are no level transitions. In such case energy is consumed only during the level transitions due to cross-conduction losses and due to the parasitic capacitance at the MOSFET output. Efficiency of pulser was evaluated using the energy consumption per pulse criteria for several load conditions. It was calculated using the high voltage supply power consumed P_{HV}, burst repetition frequency PRF, number of pulses N in a burst

$$E_{pp} = \frac{P_{HV}}{PRF \times N}. \quad (4)$$

Energy per pulse energy consumption for 200 V output at 1 nF, 50 Ω load and unloaded condition for two MOSFET types is presented in Fig. 9.

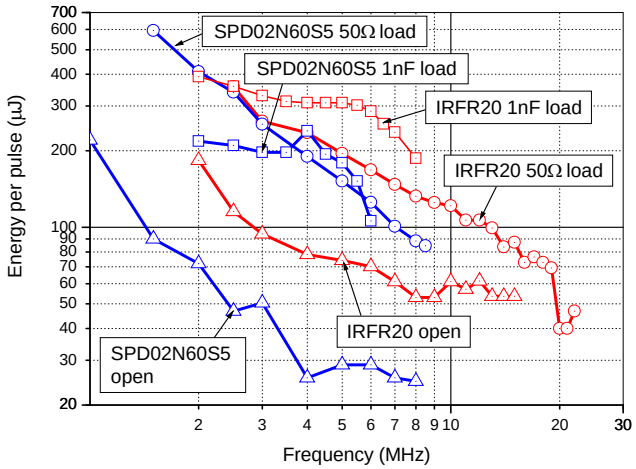

Fig. 9. Energy per pulse consumption under several load conditions.

It can be seen that higher drain peak current of IRFR20

(8 A vs. 3 A) allows higher operation frequency. Yet reduced peak current of the SPD02N60S5 gives tenfold reduction in power losses.

IV. RECEIVING ELECTRONICS

Low noise variable gain amplifier AD8031 was used in reception channel. Receiving electronics define the reception performance of the whole system. Total system gain is 80 dB with operation bandwidth 0.5 MHz to 25 MHz.

A. System AC Response

System AC response (Fig. 10) was obtained using same SWC technique. Input was fed by harmonic signal from direct digital synthesizer, driven by the clock source derived from the ADC channel. Signal at the input u_{in} was registered by ADC1 (Fig. 3) and the output signal u_{out} was connected to channel ADC2. Taking the ratio of two complex voltages the complex amplifier gain was obtained. Output AC response u_{out} was divided by input AC response u_{in}

$$G(f)=\frac{u_{out}(f)}{u_{in}(f)}. \quad (5)$$

For this type of measurements Hamming window was used instead of rectangular window: it was complicated to match exact number of periods of the fundamental frequency into analysis window. It can be seen that operation range is slightly reduced at maximum gain.

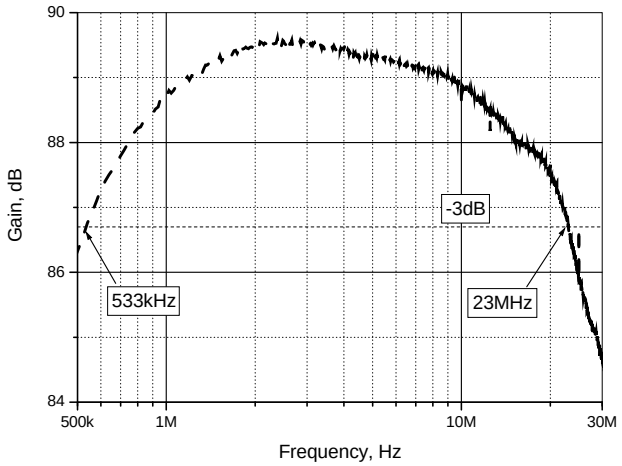

Fig. 10. System AC response at maximum gain setting.

Preamplifier parameters are essential for reception performance so it was investigated separately.

B. Receiver Noise Evaluation

System output was sampled by ADC in order to investigate reception channel noise. Record of 32 k samples was taken thousand times with passive component connected at the system input (open, 150 Ω resistor, and shorted or 0 Ω resistor). Fourier transform has been used to obtain the noise power spectral density

$$nPSD_k=\frac{2\sum_{c=1}^{C_{\max}}\left|\sum_{n=0}^{N-1}s_n e^{-i\frac{2\pi}{N}nk}\right|^2}{f_s C_{\max} N G_{sys}}=\frac{nPSD_{ADC}}{G_{sys}}. \quad (6)$$

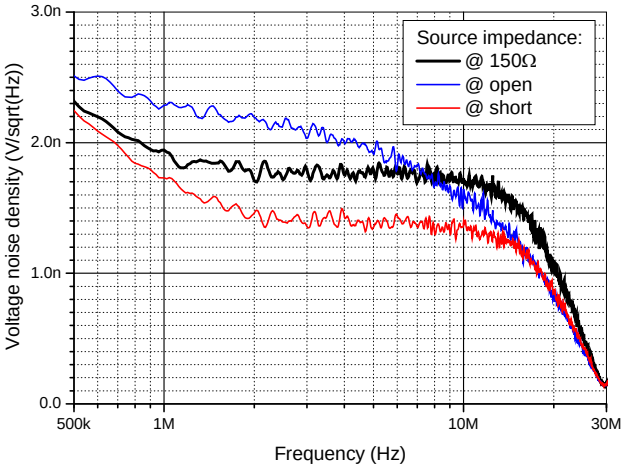

Fig. 11. Input-referred noise voltage density of the system.

Obtained noise power spectral density nPSD was power-wise averaged, divided by gain AC response (Fig. 10) and square root taken to obtain the statistical voltage noise density estimate at the system input (Fig. 11).

Noise measurements confirm that input voltage noise in case of 150 Ω signal source is 2 nV/√Hz.

C. Preamplifier Input Impedance

Preamplifier input impedance was designed for 1 kΩ using active impedance matching (R3, Fig. 12).

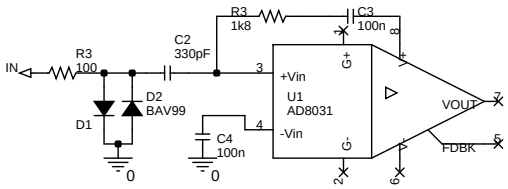

Fig. 12. Preamplifier input circuit topology with active input matching.

Parasitic capacitances of the layout and ICs will distort the situation. In order to confirm that design has reached targeted input impedance, preamplifier input impedance measurements were carried out using the technique described in [19] (Fig. 13).

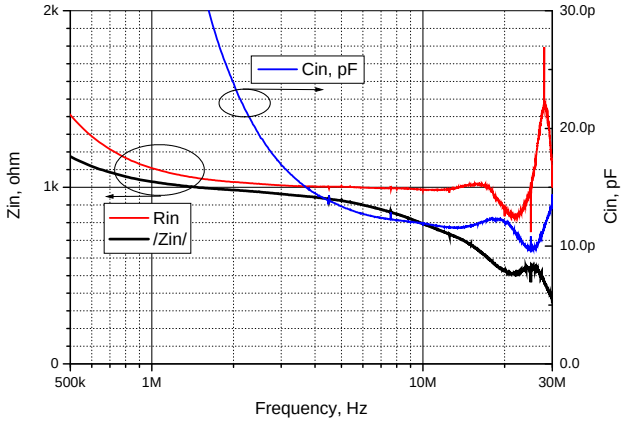

Fig. 13. Preamplifier input impedance AC response.

It can be seen that input impedance is 1 kΩ and stable within passband. Parasitic input capacitance slightly reduces input impedance magnitude at frequencies beyond 10 MHz.

D. Preamplifier Input Protection

Preamplifier input is exposed to high voltage pulses [21].

Hard diode limiter input protection was used (Fig. 14).

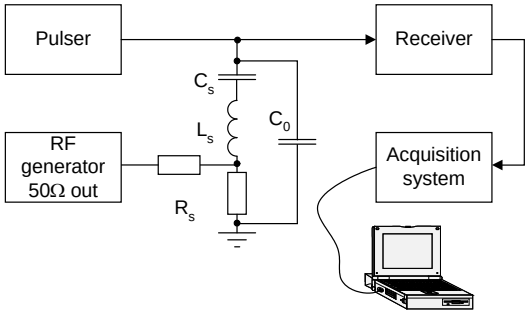

Fig. 14. Preamplifier recovery time measurement circuit.

Recovery time of the ultrasonic preamplifier is important if signal's acquisition is carried out in close vicinity of the transducer face [22].

Recovery time was estimated using technique described in [23]: i) preamplifier input was fed with sinusoidal signal via electrical model of the ultrasonic transducer, ii) system output response (Fig. 15) was registered while driving the input by rectangular high voltage pulse.

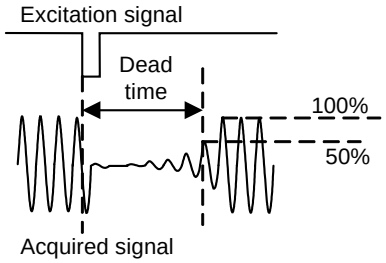

Fig. 15. Explanatory time diagrams of the recovery time measurement.

When excitation signal appears at the receiver input then preamplifier circuit is saturated and no CW signal is present at the receiver output. After excitation pulse is removed, circuit starts to recover from saturation and CW signal amplitude starts growing (Fig. 16).

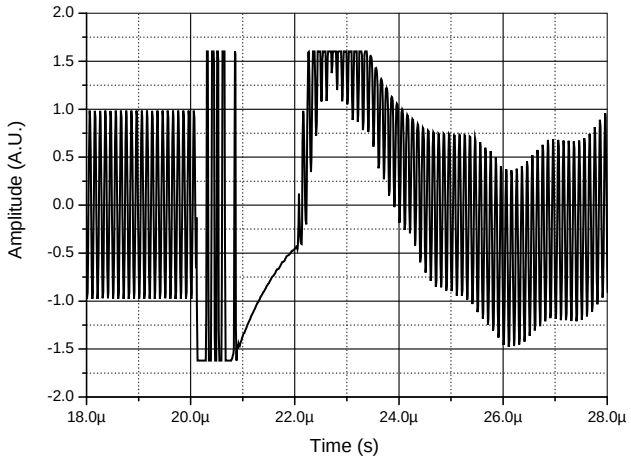

Fig. 16. Signal at the system output during the excitation pulse.

Dead time was estimated by noting the time instant when signal level is crossing the predetermined threshold level. Recorded signal was filtered to remove low frequency components. Bandpass (BP) filter equal to 100 % of the transducer bandwidth was used to extract the component of the fundamental frequency. Hilbert transform was used to obtain the envelope

$$|s_k| = \left| IDFT \begin{pmatrix} 2 \times (DFT(s_k)), \mu \geq 0 \\ 0, \mu < 0 \end{pmatrix} \right|, \quad (7)$$

where DFT and IDFT are discrete forward and inverse Fourier transform respectively, as defined in (3).

Envelope was used for recovery time estimation at -5 %–10 %, -3 dB and -50 % convergence threshold (Fig. 17).

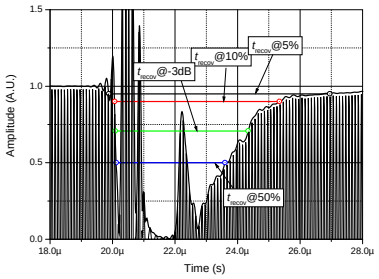

Fig. 17. Signal used for preamplifier recovery time estimation.

Recovery time was estimated as 2.5 µs at -5 % level 2.3 µs at -10 % level and 2.1 µs at -3 dB level.

V. SIGNAL DIGITIZATION ELECTRONICS

The ability to process the ultrasonic signal digitally is offering multiple advantages. Transformation of the signal into digital domain alters signal content. Noise component at reception channel output e_{ntotAout} (ADC input) has to be augmented to account the quantization noise e_{nQ} and reference clock jitter noise e_{nJ} [24]

$$e_{ntot}^{\ 2} = e_{ntotAout}^{\ 2} + e_{nQ}^{\ 2} + e_{nJ}^{\ 2}. \quad (8)$$

In [24] it was shown that if expected electronics noise at reception channel output e_{ntotAout} is 180 nV/√Hz (output noise of AD8031 at minimum gain) then no more than 20 ps jitter clock is required to avoid the clock jitter noise influence. In order to make the quantization noise influence insignificant the resolution of ADC has to be above 9 bits at 100 MHz sampling frequency.

Time of flight (ToF) estimation variance was used as optimization criteria in further analysis. Subsample interpolation case was considered. It was shown [25] that interpolation bias error exists in ToF subsample estimation if truncated interpolation function is used. For cosine [25] interpolation this error is

$$\max\left[£(ToF_c)\right] = \sqrt{®}\,\frac{2}{f_s^3}. \quad (9)$$

And for parabolic interpolation it is

$$\max\left[£(ToF_p)\right] = \max\left[£(ToF_c)\right] + \frac{f_0^2}{\sqrt{2}\,f_s^3}. \quad (10)$$

From (9) and (10) it follows that interpolation errors are influenced by signal parameters (envelope bandwidth and center frequency f_0) and sampling frequency.

ToF estimation random errors that are caused by noise can

be estimated using Cramer-Rao lower error bound

$$\pm(TOF) \geq \frac{1}{2\pi F_e \sqrt{SNR}}, \quad (11)$$

where $SNR = \frac{2E}{N_0}$, E is signal energy, F_e is effective bandwidth of the signal and N_0 is the noise power density. With signal and noise measurements available, equations (9) (10) and (11) can be reversed to derive the minimum sampling frequency. In case of cosine interpolation it is

$$f_{s\_\min\_\cos} \geq \sqrt[3]{\sqrt{18\pi^3} \times \ ^2F_e \sqrt{SNR}}. \quad (12)$$

In [25] it was shown that if signal-to-noise ratio is highest possible (180 nV/√Hz output noise of the reception channel) then minimum sampling frequency should be 67 MHz for pulse and 101 MHz for wideband chirp. Combining all the analysis 100 MHz 10 bit ADC AD9214BRSZ-105 was chosen with clock oscillator ASEMPC (3 ps jitter). Such acquisition configuration ensures that digitization errors are kept below random errors defined by analog components and 9 ps ToF uncertainty can be achieved in measurements.

VI. CONCLUSIONS

Design of ultrasonic imaging system electronics was presented. System allows exciting and collecting signals in (0.5 … 25) MHz range. Excitation signal voltage can reach ±200 V. Input impedance was designed 1 kΩ using active impedance matching. Input impedance was confirmed by measurements. System input noise is low: measurements indicate that input voltage noise density in case of 150 Ω signal source is 2 nV/√Hz. Recovery time was estimated as 2.1 μs at -3 dB threshold level. Modular design offers configuration flexibility: both single and multichannel configurations are available. Acquisition parameters are optimized.

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