Hot Interconnects and Debates on Computer Architecture Research Directions

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Welcome to the July/August 2016 issue, which contains two special features—articles on hot interconnects and debates on computer architecture research directions.

The IEEE Symposium on High Performance Interconnects has a 20-plus-year history of being a premier academic venue for the debut of the latest high-performance networking hardware. Of specific interest to *IEEE Micro*'s readership are papers targeting the high-performance computing and big data/cloud computing domains. Ryan Grant and Ada Gavrilovska are guest editors of this special issue, and they did a fantastic job selecting four interesting papers from Hot Interconnects 2015 for this special issue. I wholeheartedly thank Ryan and Ada for doing such a wonderful job. See their guest editorial for an introduction to the selected articles.

This issue also features two debate transcripts from the fourth Workshop on Computer Architecture Research Directions (CARD), held in conjunction with the International Symposium on Computer Architecture (ISCA) in June 2015 in Portland, Oregon. The CARD concept is to set up minipanels with three experts in the field, two serving as panelists and the third as a moderator. The purpose of the panel discussion is to debate the state of the field and discuss future directions. The organizers of the CARD workshop, Derek Chiou, Resit Sendag, and Joshua J. Yi, along with the panelists, then compiled transcripts of these CARD debates, which you can find in this issue. I want to thank Derek, Resit, and Josh, as well as the panelists and moderators involved for their excellent contribution.

The first CARD debate is about the impact of future technologies on architecture, with panelists Fred Chong and Igor Markov, and Trevor Mudge as the moderator. The panelists discuss the future of quantum computing, carbon nanotubes, on-chip optical interconnects, approximate computing, and new memory technologies and how these emerging technologies and directions affect processor architecture.

The second CARD debate, about proprietary versus open instruction sets, was moderated by Mark Hill, with Dave Christie and David Patterson as its panelists. Several interesting and insightful viewpoints and opinions were expressed on a topic that I'm sure will generate more discussion in the years to come.

Finally, Onur Mutlu and Rich Belgard introduce additional retrospectives of the Test of Time Awards of the International Symposium on Microarchitecture (MICRO). These awards recognize the most influential papers published in past MICRO conferences that have had significant impact in the field. We included two retrospectives in the Jan./Feb. 2016 issue; this issue includes four more:

- Thomas Gross and colleagues discuss the paper "MIPS: A Microprocessor Architecture."
- Yale Patt and colleagues discuss their three awarded papers on the HPS microarchitecture: "HPS, A New Microarchitecture: Rationale and Introduction," "Critical Issues Regarding HPS, A High Performance Microarchitecture," and "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines."
- Tse-Yu Yeh and Yale Patt discuss the paper "Two-Level Adaptive Training Branch Prediction."
- Andy Wolfe discusses the paper "Executing Compressed Programs on an Embedded RISC Architecture," coauthored with Alex Chanin.

I congratulate the award winners, and I hope you will enjoy reading these retrospectives as much as I did. As always, I wish you happy reading!

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