IEEE Design & Test

Call for Papers

Special Issue on "Speeding up Analog Integration and Test for Mixed-signal SOCs"

Publication Date: January 2015 (likely)

Today's integrated circuits with embedding processing capabilities have an ever increasing analog content. While this helps to build richer end applications easily, it significantly complicates the design process. A gamut of heterogeneous analog and digital functional modules must now be integrated across different voltage levels and interfaces. Analog integration and test is hence emerging as perhaps the biggest challenge in an otherwise standard SOC (system-on-chip) design flow. This special issue will cover advances in test and verification of analog, mixed-signal and RF circuits and systems, both in theory and practice.

Papers are solicited in different areas describing new techniques as well as adoption challenges in known ones. These include topics in automation and CAD (algorithmic approaches, modeling methods and abstractions, application of formal methods), circuits and design (new design ideas – complex high speed I/Os, BIST IPs, on-chip calibration and test methods), integration and verification (overlaying power management functions and different operating modes, FPGA based prototyping, improvements over mixed-mode simulation), test methodology (specification tests and alternatives, adaptive analog test), test technology and test cost (tester infrastructure, test application challenges, managing co-existence between multiple analog / digital modules, rapid silicon bring-up, higher multi-site challenges, manufacturing test optimizations, test cost reduction), and emerging areas (e.g. integration and test of sensor IPs and cognitive radios, online test requirements for analog modules in critical applications, 3D analog integration).

While there is distributed standalone material in the literature on some of these topics, this special issue will serve as a compendium of articles reflecting the state-of-the-art, with special focus on design and implementation techniques for mixed-signal SOCs. Directional and survey papers are also welcome.

Paper submission and review:

Papers are solicited in the above (and related topics). All papers must adhere to IEEE Design & Test submissions guidelines <http://www.eng.ucy.ac.cy/theocharides/ieeedt/submission.html> and must be submitted electronically to the IEEE Manuscript Central web site at <https://mc.manuscriptcentral.com/dandt> . Please indicate that the paper is being submitted for the special issue on "Speeding up Analog Integration and Test for Mixed-signal SOCs". All submitted papers will be undergoing the regular IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Accepted articles will be edited for structure, grammar, readability, and adherence to IEEE Design & Test print format.

Timelines for submissions, reviews and final paper preparation:

(a) Papers due for review : March 15, 2014.
(b) Reviews complete and notification : May 15, 2014.
(c) Revised papers due : June 15, 2014.
(d) Notification of final acceptance : July 15, 2014.
(e) Final papers (as per D&T guidelines) : August 15, 2014.
(f) Publication date : January 2015 (likely)

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